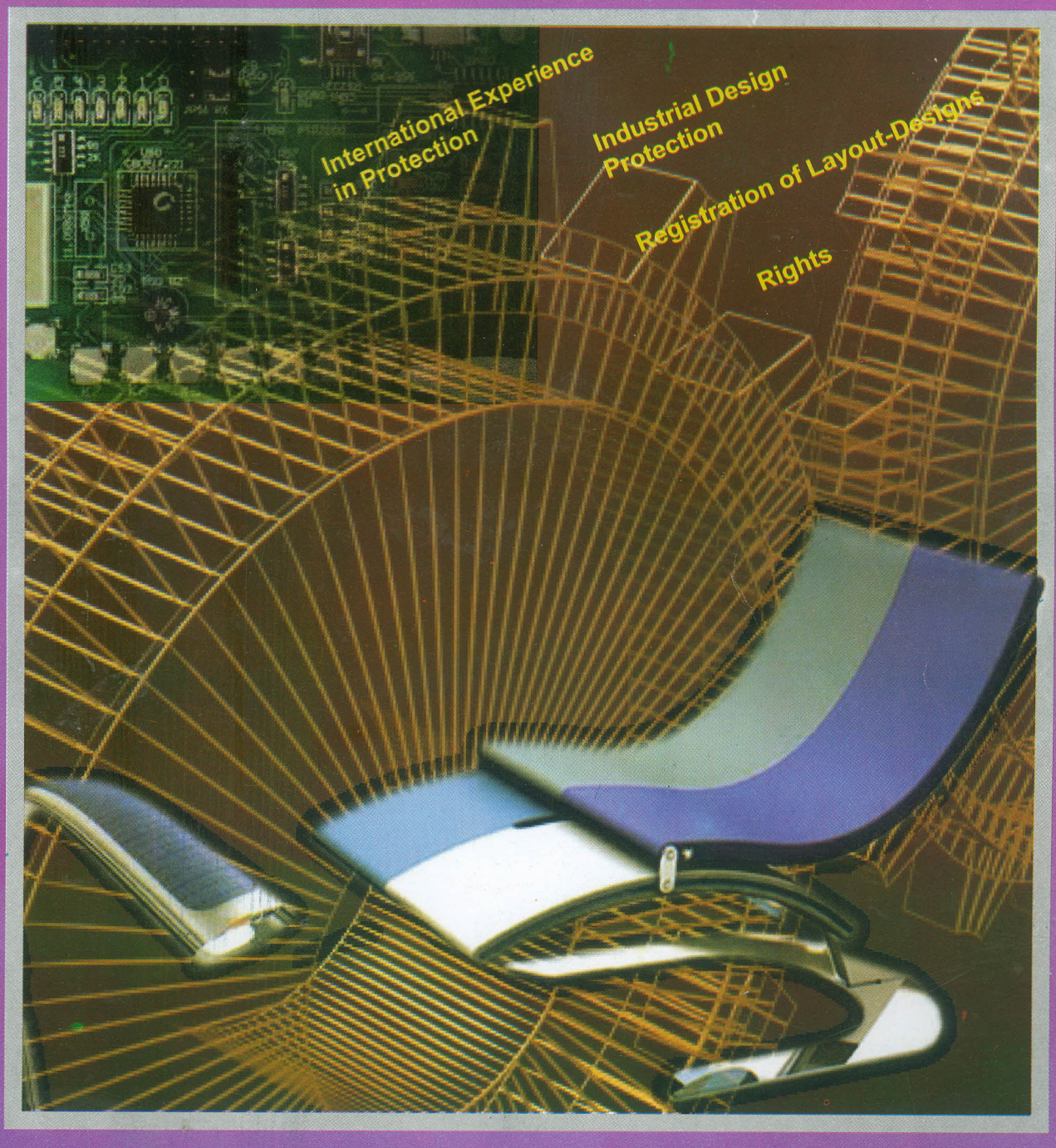
ignou
THE PEOPLE'S
UNIVERSITY

Indira Gandhi National Open University
School of Law

MIP-103
INDUSTRIAL DESIGNS AND LAYOUT DESIGNS OF INTEGRATED CIRCUITS AND UTILITY MODELS



Layout-Designs of Semiconductor Integrated Circuits

2

"शिक्षा मानव को बन्धनों से मुक्त करती है और आज के युग में तो यह लोकतंत्र की भावना का आधार भी है। जन्म तथा अन्य कारणों से उत्पन्न जाति एवं वर्गगत विषमताओं को दूर करते हुए मनुष्य को इन सबसे ऊपर उठाती है।"

— *इन्दिरा गांधी*

"Education is a liberating force, and in our age it is also a democratising force, cutting across the barriers of caste and class, smoothing out inequalities imposed by birth and other circumstances."

– Indira Gandhi

Indira Gandhi
National Open University
School of Law

MIP-103
Industrial Designs and Layout Designs of Integrated Circuits and Utility Models

Block

2

LAYOUT-DESIGNS OF SEMICONDUCTOR INTEGRATED CIRCUITS

UNIT 5

Basics on Integrated Circuits and Scope of Legal Protection 5

UNIT 6

Registration of Layout-Designs of Semiconductor ICs 23

UNIT 7

Rights Acquired by Registration of Integrated Circuits 40

Expert Committee

Dr. D.P.S Parmar
Technical Member,
Intellectual Property Appellate Board,
Ministry of Commerce & Industry

Prof. S.K. Verma
Director, ISIL
New Delhi

Prof. Salim Akhtar
Professor of Law,
Aligarh Muslim University
Aligarh, Uttar Pradesh

Dr. Ekbal Hussain
Associate Professor
Jamia Milia Islamia University
New Delhi

Mr. T.C. James
Director,
National Intellectual Property Organisation
New Delhi

Prof. K. Elumalai
Director, School of Law
IGNOU

Dr. Suneet Kashyap Srivastava
Assistant Professor, School of Law
IGNOU

Dr. Gurmeet Kaur
Assistant Professor, School of Law
IGNOU

Mr. Anand Gupta
Assistant Professor, School of Law
IGNOU

Ms. Mansi Sharma
Assistant Professor, School of Law
IGNOU

Programme Coordinator: Dr. Suneet Kashyap Srivastava
School of Law, IGNOU, New Delhi

Block Prepration Team

Unit Writer:
Mr. K. Subodh Kumar
Former Head
Andhra Pradesh Technology
Development and Promotion
Centre

Content Editor
Mr. T.C. James
Head
National Institute of Intelletual
Property Organisation (NIPO)
New Delhi

Format & Language Editor:
Dr. Suneet K. Srivastava
SOL, IGNOU, New Delhi

Print Production :

S. Burman, DR (P)	**Tilakraj, AR (P)**	**Yashpal, SO (P)**
MPDD (IGNOU)	MPDD (IGNOU)	MPDD (IGNOU)

March, 2017 (Reprint)
© Indira Gandhi National Open University, 2013

ISBN : 978-81-266-6265-4

All rights reserved. No part of this work may be reproduced in any form, by mimeograph or any other means, without permission in writing from the Indira Gandhi National Open University.

Further information on the Indira Gandhi National Open University courses may be obtained from the University's office at Maidan Garhi, New Delhi-110 068.
Printed and Published on behalf of the Indira Gandhi National Open University, New Delhi by Registrar, MPDD.
Printed at : Laxmi Printindia-556 G.T. Road Shahadra, Delhi-32

BLOCK 2 LAYOUT-DESIGNS OF SEMICONDUCTOR INTEGRATED CIRCUITS

Layout Designs of Semiconductor Integrated Circuts.

Block 2 of this Course is divided into three units. This Block extensively deals with layout designs of semiconductor and integrated circuits.

Unit 5 : The **Unit 5** of this block deals with the basics on integrated circuits and the scope of legal protection.

Unit 6 : The **Unit 6** of this block deals with the registration procedure of layout designs of semiconductor and integrated circuits.

Unit 7 : The **Unit 7** of this block deals with those rights which are acquired through the registration of integrated circuits.

UNIT 5 BASICS ON INTEGRATED CIRCUITS AND SCOPE OF LEGAL PROTECTION

Structure

5.1 Introduction

5.2 Objectives

5.3 Landmark Inventions in Integrated Circuits

5.4 Key developments in IC Technology

5.5 Classification of Integrated Circuits

5.6 Fabrication

5.7 Packaging

5.8 Protection of Semiconductor Chips Layout-Design

5.9 Case Studies and Example of Integrated Circuits

5.10 Summary

5.11 Terminal Questions

5.12 Answers and Hints

5.13 References and Suggested Readings

5.1 INTRODUCTION

An **integrated circuit** or **monolithic integrated circuit** (also referred to as **IC**, **chip**, or **microchip**) is an electronic circuit manufactured by the patterned diffusion of trace elements into the surface of a thin substrate of semiconductor material. Additional materials are deposited and patterned to form interconnections between semiconductor devices.

Integrated circuits are used in virtually all electronic equipment today and have revolutionised the world of electronics. Computers, mobile phones, and other digital appliances are now inextricable parts of the structure of modern societies, made possible by the low cost of production of integrated circuits.

IC was made possible by experimental discoveries showing that Semiconductor devices could perform the functions of vacuum tubes and by mid-20th-century technology advancements in Semiconductor device fabrication. The integration of large numbers of tiny transistors into a small chip was an enormous improvement over the manual assembly of circuits using discrete electronic components. The integrated circuit's mass production capability, reliability, and building-block approach to circuit design ensured the rapid adoption of standardised ICs in place of designs using discrete transistors.

There are two main advantages of ICs over discrete circuits: cost and performance. Cost is low because the chips, with all their components, are printed as a unit by photolithography rather than being constructed one transistor at a time. Furthermore,

much less material is used to construct a packaged IC die than to construct a discrete circuit. Performance is high because the components switch quickly and consume little power (compared to their discrete counterparts) as a result of the small size and close proximity of the components. As of 2006, typical chip areas range from a few square millimetres to around 350 mm^2, with up to 1 million transistors per mm^2.

> *Integrated circuit* originally referred to a miniaturised electronic circuit consisting of semiconductor devices, as well as passive components bonded to a substrate or circuit board. This configuration is now commonly referred to as a hybrid integrated circuit. *Integrated circuit* has since come to refer to the single-piece circuit construction originally known as a *monolithic integrated circuit*.

5.2 OBJECTIVES

After reading this unit, you should be able to:

- explain the basic concepts of integrated circuts;
- describe the key inventions and the scope of protection of integrated circuits through intellectual property rights; and
- explain the nature and scope of protection.

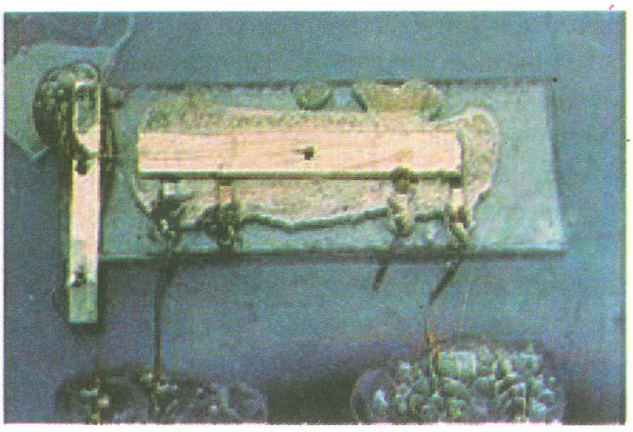
5.3 LANDMARK INVENTIONS IN INTEGRATED CIRCUITS

Early developments of the integrated circuit go back to 1949, when the German engineer Werner Jacobi (Siemens AG) filed a patent for an integrated-circuit-like semiconductor amplifying device showing five transistors on a common substrate arranged in a 2-stage amplifier arrangement. Jacobi disclosed small and cheap hearing aids as typical industrial applications of his patent. A commercial use of his patent has not been reported.

The idea of the integrated circuit was conceived by a radar scientist working for the Royal Radar Establishment of the British Ministry of Defence, Geoffrey W.A. Dummer (1909–2002). Dummer presented the idea to the public at the Symposium on Progress in Quality Electronic Components in Washington, D.C. on May 7, 1952. He gave many symposia publicly to propagate his ideas, and unsuccessfully attempted to build such a circuit in 1956.

A precursor idea to the IC was to create small ceramic squares (wafers), each one containing a single miniaturised component. Components could then be integrated and wired into a bi-dimensional or tri-dimensional compact grid. This idea, which looked very promising in 1957, was proposed to the US Army by Jack Kilby, and led to the short-lived Micromodule Program. However, as the project was gaining momentum, Kilby came up with a new, revolutionary design: the IC.

Robert Noyce credited Kurt Lehovec of Sprague Electric for the *principle of p-n junction isolation* caused by the action of a biased p-n junction (the diode) as a key concept behind the IC.



Jack Kilby's original integrated circuit[1]

Newly employed by Texas Instruments, Kilby recorded his initial ideas concerning the integrated circuit in July 1958, successfully demonstrating the first working integrated example on September 12, 1958. In his patent application of February 6, 1959, Kilby described his new device as "a body of Semiconductor material ... wherein all the components of the electronic circuit are completely integrated." Kilby won the 2000 Nobel Prize in Physics for his part of the invention of the integrated circuit. Kilby's work was named an IEEE Milestone in 2009.

Noyce also came up with his own idea of an integrated circuit half a year later than Kilby. His chip solved many practical problems that Kilby's had not. Produced at Fairchild Semiconductor, it was made of silicon, whereas Kilby's chip was made of germanium.

Fairchild Semiconductor was also home of the first silicon gate IC technology with self-aligned gates, which stands at the basis of all modern CMOS computer chips. The technology was developed by Italian physicist Federico Faggin in 1968, who later joined Intel in order to develop the very first Central Processing Unit (CPU) on one chip (Intel 4004), for which he received the National Medal of Technology and Innovation in 2010.

5.4 KEY DEVELOPMENTS IN IC TECHNOLOGY

In the early days of integrated circuits, only a few transistors could be placed on a chip, as the scale used was large because of the contemporary technology, and manufacturing yields were low by today's standards. As the degree of integration was small, the design was done easily. Over time, millions, and today billions, of transistors could be placed on one chip, and to make a good design became a task to be planned thoroughly. This gave rise to new design methods.

The first integrated circuits contained only a few transistors. Called "**small-scale integration**" (**SSI**), digital circuits containing transistors numbering in the tens provided a few logic gates for example, while early linear ICs such as the Plessey SL201 or the Philips TAA320 had as few as two transistors. The term Large Scale Integration was first used by IBM scientist Rolf Landauer when describing the theoretical concept, from there came the terms for SSI, MSI, VLSI, and ULSI.

SSI circuits were crucial to early aerospace projects, and aerospace projects helped inspire development of the technology. Both the Minuteman missile and

[1] Source : www.nobelprize.org

Apollo program needed lightweight digital computers for their inertial guidance systems; the Apollo guidance computer led and motivated the integrated-circuit technology, while the Minuteman missile forced it into mass-production. The Minuteman missile program and various other Navy programs accounted for the total $4 million integrated circuit market in 1962, and by 1968, U.S. Government space and defence spending still accounted for 37% of the $312 million total production. The demand by the U.S. Government supported the nascent integrated circuit market until costs fell enough to allow firms to penetrate the industrial and eventually the consumer markets. The average price per integrated circuit dropped from $50.00 in 1962 to $2.33 in 1968. Integrated circuits began to appear in consumer products by the turn of the decade, a typical application being FM inter-carrier sound processing in television receivers.

The next step in the development of integrated circuits, taken in the late 1960s, introduced devices which contained hundreds of transistors on each chip, called "**medium-scale integration**" (**MSI**).

They were attractive economically because while they cost little more to produce than SSI devices, they allowed more complex systems to be produced using smaller circuit boards, less assembly work (because of fewer separate components), and a number of other advantages.

Further development, driven by the same economic factors, led to "**large-scale integration**" (**LSI**) in the mid-1970s, with tens of thousands of transistors per chip.

Integrated circuits such as 1K-bit RAMs, calculator chips, and the first microprocessors, that began to be manufactured in moderate quantities in the early 1970s, had under 4000 transistors. True LSI circuits, approaching 10,000 transistors, began to be produced around 1974, for computer main memories and second-generation microprocessors.

Among the most advanced integrated circuits are the microprocessors or "**cores**", which control everything from computers and cellular phones to digital microwave ovens. Digital memory chips and ASICs are examples of other families of integrated circuits that are important to the modern information society. While the cost of designing and developing a complex integrated circuit is quite high, when spread across typically millions of production units the individual IC cost is minimised. The performance of ICs is high because the small size allows short traces which in turn allows low power logic (such as CMOS) to be used at fast switching speeds.

ICs have consistently migrated to smaller feature sizes over the years, allowing more circuitry to be packed on each chip. This increased capacity per unit area can be used to decrease cost and/or increase functionality — see Moore's law which, in its modern interpretation, states that the number of transistors in an integrated circuit doubles every two years. In general, as the feature size shrinks, almost everything improves — the cost per unit and the switching power consumption go down, and the speed goes up. However, ICs with nanometer-scale devices are not without their problems, principal among which is leakage current, although these problems are not insurmountable and will likely be solved or at least ameliorated by the introduction of high-k dielectrics. Since these speed and power consumption gains are apparent to the end user, there is fierce competition among the manufacturers to use finer geometries.

In current research projects, integrated circuits are also developed for sensoric applications in medical implants or other bioelectronics devices. Particular sealing strategies have to be taken in such biogenic environments to avoid corrosion or biodegradation of the exposed Semiconductor materials. As one of the few materials well established in CMOS technology, titanium nitride (TiN) turned out as exceptionally stable and well suited for electrode applications in medical implants.

5.5 CLASSIFICATION OF INTEGRATED CIRCUITS

Integrated circuits can be classified into analog, digital and mixed signal (both analog and digital on the same chip).

Digital integrated circuits can contain anything from one to millions of logic gates, flip-flops, multiplexers, and other circuits in a few square millimetres. The small size of these circuits allows high speed, low power dissipation, and reduced manufacturing cost compared with board-level integration. These digital ICs, typically microprocessors, DSPs, and micro controllers, work using binary mathematics to process "one" and "zero" signals.

Analog ICs, such as sensors, power management circuits, and operational amplifiers, work by processing continuous signals. They perform functions like amplification, active filtering, demodulation, and mixing. Analog ICs ease the burden on circuit designers by having expertly designed analog circuits available instead of designing a difficult analog circuit from scratch.

ICs can also combine analog and digital circuits on a single chip to create functions such as A/D converters and D/A converters. Such circuits offer smaller size and lower cost, but must carefully account for signal interference.

5.6 FABRICATION

Semiconductor ICs are fabricated in a layer process which includes these key process steps:

- Imaging
- Deposition
- Etching

The main process steps are supplemented by doping and cleaning.

Mono-crystal silicon wafers (or for special applications, silicon on sapphire or gallium arsenide wafers) are used as the *substrate*. Photolithography is used to mark different areas of the substrate to be doped or to have polysilicon, insulators or metal (typically aluminium) tracks deposited on them.

Integrated circuits are composed of many overlapping layers, each defined by photolithography, and normally shown in different colours. Some layers mark where various dopants are diffused into the substrate (called diffusion layers), some define where additional ions are implanted (implant layers), some define the conductors (polysilicon or metal layers), and some define the connections between the conducting layers (via or contact layers). All components are constructed from a specific combination of these layers.

In a self-aligned CMOS process, a transistor is formed wherever the gate layer (polysilicon or metal) crosses a diffusion layer.

Capacitive structures, in form very much like the parallel conducting plates of a traditional electrical capacitor, are formed according to the area of the "plates", with insulating material between the plates. Capacitors of a wide range of sizes are common on ICs.

Meandering stripes of varying lengths are sometimes used to form on-chip resistors, though most logic circuits do not need any resistors. The ratio of the length of the resistive structure to its width, combined with its sheet resistivity, determines the resistance.

More rarely, inductive structures can be built as tiny on-chip coils, or simulated by gyrators.

Since a CMOS device only draws current on the *transition* between logic states, CMOS devices consume much less current than bipolar devices.

A random access memory is the most regular type of integrated circuit; the highest density devices are thus memories; but even a microprocessor will have memory on the chip.

Although the structures are intricate – with widths which have been shrinking for decades – the layers remain much thinner than the device widths. The layers of material are fabricated much like a photographic process, although light waves in the visible spectrum cannot be used to "expose" a layer of material, as they would be too large for the features. Thus photons of higher frequencies (typically ultraviolet) are used to create the patterns for each layer. Because each feature is so small, electron microscopes are essential tools for a process engineer who might be debugging a fabrication process.

Each device is tested before packaging using automated test equipment (ATE), in a process known as wafer testing, or wafer probing. The wafer is then cut into rectangular blocks, each of which is called a *die*. Each good die (plural *dice*, *dies*, or *die*) is then connected into a package using aluminium (or gold) bond wires which are welded and/or thermosonic bonded to *pads*, usually found around the edge of the die. After packaging, the devices go through final testing on the same or similar ATE used during wafer probing. Industrial CT scanning can also be used. Test cost can account for over 25% of the cost of fabrication on lower cost products, but can be negligible on low yielding, larger, and/or higher cost devices.

As of 2005, a fabrication facility (commonly known as a *semiconductor fab*) costs over $1 billion to construct, because much of the operation is automated. Today, the most advanced processes employ the following techniques:

- The wafers are up to 300 mm in diameter (wider than a common dinner plate).
- Use of 32 nanometre or smaller chip manufacturing process. Intel, IBM, NEC, and
- AMD are using ~32 nanometres for their CPU chips. IBM and AMD introduced immersion lithography for their 45 nm processes.
- Copper interconnects where copper wiring replaces aluminium for interconnects.

- Low-K dielectric insulators.
- Silicon on insulator (SOI)
- Strained silicon in a process used by IBM known as strained silicon directly on insulator (SSDOI)
- Multigate devices such as tri-gate transistors being manufactured by Intel from 2011 in their 22 nm process.

5.7 PACKAGING

The earliest integrated circuits were packaged in ceramic flat packs, which continued to be used by the military for their reliability and small size for many years. Commercial circuit packaging quickly moved to the dual in-line package (DIP), first in ceramic and later in plastic. In the 1980s pin counts of VLSI circuits exceeded the practical limit for DIP packaging, leading to pin grid array (PGA) and leadless chip carrier (LCC) packages. Surface mount packaging appeared in the early 1980s and became popular in the late 1980s, using finer lead pitch with leads formed as either gull-wing or J-lead, as exemplified by small-outline integrated circuit — a carrier which occupies an area about 30–50% less than an equivalent DIP, with a typical thickness that is 70% less. This package has "gull wing" leads protruding from the two long sides and a lead spacing of 0.050 inches.

In the late 1990s, plastic quad flat pack (PQFP) and thin small-outline package (TSOP) packages became the most common for high pin count devices, though PGA packages are still often used for high-end microprocessors. Intel and AMD are currently transitioning from PGA packages on high-end microprocessors to land grid array (LGA) packages.

Ball grid array (BGA) packages have existed since the 1970s. Flip-chip Ball Grid Array packages, which allow for much higher pin count than other package types, were developed in the 1990s. In an FCBGA package the die is mounted upside-down (flipped) and connects to the package balls via a package substrate that is similar to a printed-circuit board rather than by wires. FCBGA packages allow an array of input-output signals (called Area-I/O) to be distributed over the entire die rather than being confined to the die periphery.

Traces out of the die, through the package, and into the printed circuit board have very different electrical properties, compared to on-chip signals. They require special design techniques and need much more electric power than signals confined to the chip itself.

When multiple dies are put in one package, it is called SiP, for *System In Package*. When multiple dies are combined on a small substrate, often ceramic, it's called an MCM, or Multi-Chip Module. The boundary between a big MCM and a small printed circuit board is sometimes fuzzy.

Chip labelling and manufacture date

Most integrated circuits large enough to include identifying information include four common sections: the manufacturer's name or logo, the part number, a part production batch number and/or serial number, and a four-digit code that identifies when the chip was manufactured. Extremely small surface mount technology parts often bear only a number used in a manufacturer's lookup table to find the chip characteristics.

The manufacturing date is commonly represented as a two-digit year followed by a two-digit week code, such that a part bearing the code 8341 was manufactured in week 41 of 1983, or approximately in October 1983.

Self Assessment Question **(Spend 3 minutes)**

1) List down your key learning Points on IC Circuits.

.....

.....

.....

.....

5.8 PROTECTION OF SEMI CONDUCTOR CHIPS LAYOUT-DESIGN

Like most of the other forms of intellectual property, IC layout designs are creations of the human mind. They are usually the result of an enormous investment, both in terms of the time of highly qualified experts, and financially. There is a continuing need for the creation of new layout-designs which reduce the dimensions of existing integrated circuits and simultaneously increase their functions. The smaller an integrated circuit, the less the material needed for its manufacture, and the smaller the space needed to accommodate it. Integrated circuits are utilised in a large range of products, including articles of everyday use, such as watches, television sets, washing machines, automobiles, etc., as well as sophisticated data processing equipment.

The possibility of copying by photographing each layer of an integrated circuit and preparing photomasks for its production on the basis of the photographs obtained is the main reason for the introduction of legislation for the protection of layout-designs.

Article 35 of the TRIPS Agreement requires Member countries to protect the layout-designs of integrated circuits in accordance with the provisions of the IPIC Treaty (the Treaty on Intellectual Property in Respect of Integrated Circuits), negotiated under the auspices of WIPO in 1989. These provisions deal with, *inter alia*, the definitions of "integrated circuit" and "layout-design (topography)", requirements for protection, exclusive rights, and limitations, as well as exploitation, registration and disclosure.

An "integrated circuit" means a product, in its final form or an intermediate form, in which the elements, at least one of which is an active element, and some or all of the interconnections are integrally formed in and/or on a piece of material and which is intended to perform an electronic function.

A "layout-design (topography)" is defined as the three-dimensional disposition, however expressed, of the elements, at least one of which is an active element, and of some or all of the interconnections of an integrated circuit, or such a three-dimensional disposition prepared for an integrated circuit intended for manufacture. The obligation to protect layout-designs applies to such layout-designs that are original in the sense that they are the result of their creators' own intellectual effort

and are not commonplace among creators of layout-designs and manufacturers of integrated circuits at the time of their creation. The exclusive rights include the right of reproduction and the right of importation, sale and other distribution for commercial purposes. Certain limitations to these rights are provided for.

In addition to requiring Member countries to protect the layout-designs of integrated circuits in accordance with the provisions of the IPIC Treaty, the TRIPS Agreement clarifies and/or builds on four points. These points relate to the term of protection (ten years instead of eight, Article 38), the applicability of the protection to articles containing infringing integrated circuits (last sub clause of Article 36) and the treatment of innocent infringers (Article 37.1). The conditions in Article 31 of the TRIPS Agreement apply mutatis mutandis to compulsory or non-voluntary licensing of a layout-design or to its use by or for the government without the authorisation of the right holder, instead of the provisions of the IPIC Treaty on compulsory licensing (Article 37.2).

A diplomatic conference was held at Washington, D.C., in 1989, which adopted a Treaty on Intellectual Property in Respect of Integrated Circuits (IPIC Treaty). The Treaty on Intellectual Property in respect of Integrated Circuits, also called Washington Treaty or IPIC Treaty (signed at Washington on May 26, 1989) is currently not in force, but most of the provisions of the treay were integrated into the TRIPS agreement through Article 35 of that Agreement..

National laws protecting IC layout designs have been adopted in a number of countries.

Self Assessment Question **(Spend 3 minutes)**

2) List out the key sections of TRIPS Agreement which are relevant to IC Circuit Protection.

.....

.....

.....

.....

5.9 CASE STUDIES AND EXAMPLES OF PROTECTION OF INTEGRATED CIRCUITS

The integrated circuit controls the functions of the quartz watch.

In all quartz watches, the IC makes the quartz crystal oscillate, divides the quartz frequency down to one pulse per second, and drives the display. Many more functions can be added using a microprocessor, making today's quartz watches more like dedicated microcomputers. Both Swiss and Japanese watch companies were involved in developing ICs suitable for use in watches. The first IC used in a watch was developed in the 1960s in a Swiss laboratory, CEH. The chip's power consumption had to be drastically reduced in order to allow battery life of at least one year. In the first quartz watch, the Beta 21, a single IC containing about 110 components managed all electronic functions

of the watch, including quartz crystal excitation, frequency division, and motor drive. In 1970 the Seiko 36SQC was introduced and was the first quartz watch to use a CMOS chip (a low energy integrated circuit invented at Fairchild in 1963). Today's quartz watches all use CMOS technology, with chips containing 100,000 components and more. They combine microprocessor, memory and analog functions, and act like dedicated microcomputers.

In May 1952 Geoffrey Dummer read a paper at the US Electronic Components Symposium. At the end of the paper he made the statement:

"With the advent of the transistor and the work on Semiconductors generally, it now seems possible to envisage electronic equipment in a solid block with no connecting wires. The block may consist of layers of insulating, conducting, rectifying and amplifying materials, the electronic functions being connected directly by cutting out areas of the various layers". This is now generally accepted as the first public description of an integrated circuit.

At a later date he said, "It seemed so logical to me; we had been working on smaller and smaller components, improving reliability as well as size reduction. I thought the only way we could ever attain our aim was in the form of a solid block. You then do away with all your contact problems, and you have a small circuit with high reliability. And that is why I went on with it. I shook the industry to the bone. I was trying to make them realise how important its invention would be for the future of microelectronics and the national economy".

His ability to turn his idea of an integrated circuit into practical reality was restricted by his lack of responsibility for active devices and the lack of suitable manufacturing techniques. He got over his lack of suitable authority to commission development work by placing a small contract with Plessey under the auspices of his Constructional Techniques Group. The result was shown at The International Components Symposium he initiated at R.R.E. Malvern in September 1957, where he presented a model to illustrate the possibilities of solid-circuit techniques. The model represented a flip-flop in the form of a solid block of Semiconductor material suitably doped and shaped to form four transistors. Four resistors were represented by silicon bridges, and other resistors and capacitors were deposited in film form directly onto the silicon block with intervening insulating films. The model was intended as a design exercise, but was not too different from the circuit patented by Jack St Clair Kilby two years later.

As with many inventions, two people had the idea for an integrated circuit at almost the same time. Transistors had become commonplace in everything from radios to phones to computers, and now manufacturers wanted something even better. Sure, transistors were smaller than vacuum tubes, but for some of the newest electronics, they weren't small enough.

But there was a limit on how small you could make each transistor, since after it was made it had to be connected to wires and other electronics. The transistors were already at the limit of what steady hands and tiny tweezers could handle. So, scientists wanted to make a whole circuit – the transistors, the wires, everything else they needed – in a single blow. If they could create a miniature circuit in just one step, all the parts could be made much smaller.

One day in late July, Jack Kilby was sitting alone at Texas Instruments. He had been hired only a couple of months earlier and so he wasn't able to take vacation time when practically everyone else did. The halls were deserted, and he had lots of time to think. It suddenly occurred to him that all parts of a circuit, not just the transistor, could be made out of silicon. At the time, nobody was making capacitors or resistors out of semiconductors. If it could be done then the entire circuit could be built out of a single crystal — making it smaller and much easier to produce. Kilby's boss liked the idea, and told him to get to work. By September 12, Kilby had built a working model, and on February 6, Texas Instruments filed a patent. Their first "Solid Circuit" the size of a pencil point, was shown off for the first time in March.

But over in California, another man had similar ideas. In January of 1959, Robert Noyce was working at the small Fairchild Semiconductor startup company. He also realised a whole circuit could be made on a single chip. While Kilby had hammered out the details of making individual components, Noyce thought of a much better way to connect the parts. That spring, Fairchild began a push to build what they called "unitary circuits" and they also applied for a patent on the idea. Knowing that TI had already filed a patent on something similar, Fairchild wrote out a highly detailed application, hoping that it wouldn't infringe on TI's similar device.

All that detail paid off. On April 25, 1961, the patent office awarded the first patent for an integrated circuit to Robert Noyce while Kilby's application was still being analysed. Today, both men are acknowledged as having independently conceived of the idea.

Jack St. Clair Kilby (November 8, 1923 – June 20, 2005) was an American physicist who took part (along with Robert Noyce) in the realisation of the first integrated circuit while working at Texas Instruments (TI) in 1958. He was awarded the Nobel Prize in physics in 2000. He is also the inventor of the handheld calculator and the thermal printer.One of his key inventions is described below :

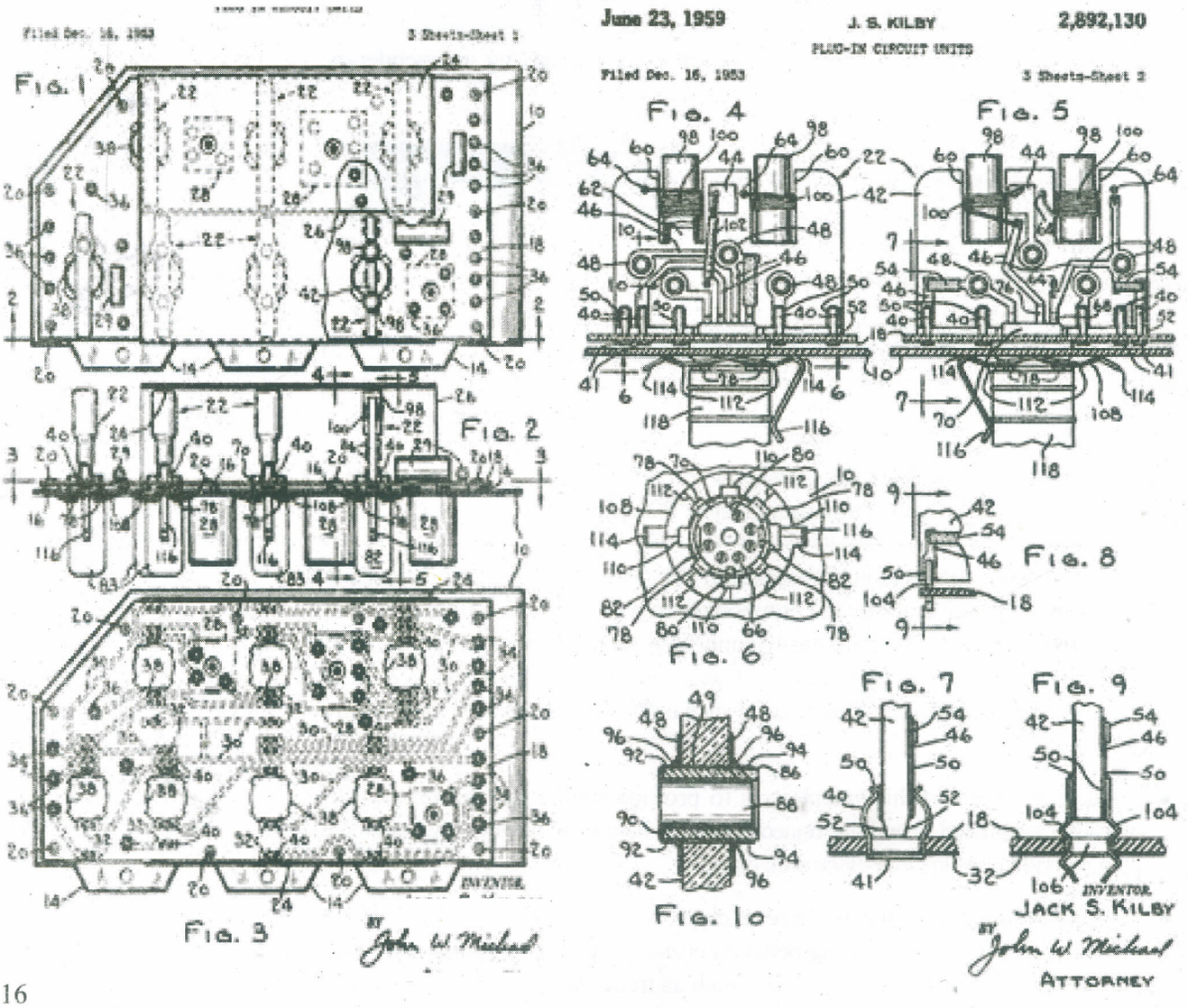
Invention 1 : Plug-IN Circuit Units		
Patented June 23, 1959		2,892,130
Jack S. Kilby, Milwaukee, Wis., assignor to Globe-Union Inc., Milwaukee, Wis., a corporation of Delaware		

- This invention relates to improvements in electrical circuit units and particularly such units which embody the components required for a single stage of an electronic circuitry and are easily connected with other such units to form complete circuits for apparatus such as radio and television receivers. It is an object of this invention to provide such a unit which may be inexpensively manufactured.
- Another object of this invention is to provide such a unit which may be readily assembled to and disconnected from a base plate having other circuitry to provide a multistage electronic circuit.
- In obtaining these objects there is employed a base plate having on its surface conductors extending between prongs or prong receiving openings. A multiplicity of single stage units, such as frequency modifiers, video and

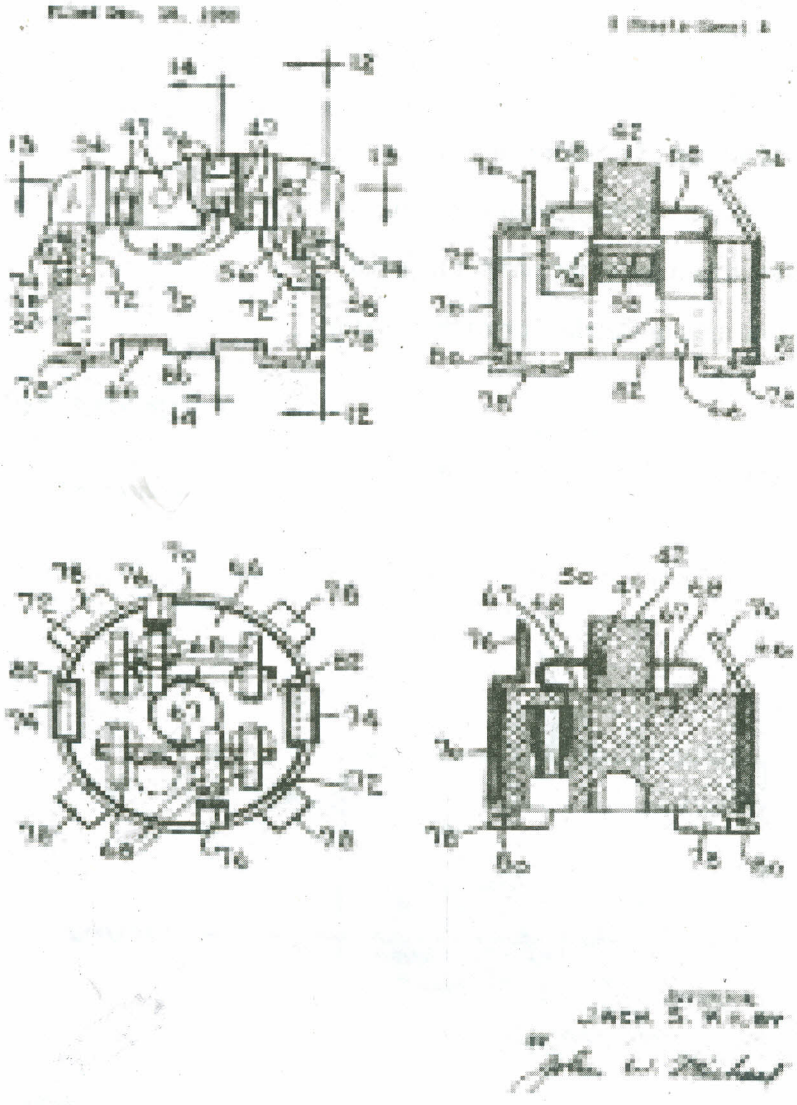
sound amplifiers, limiters and detectors are plugged into such base plate to make the complete circuit. In its general aspects each single stage unit consists of a unit plate of insulating material having on its faces capacitor plates, resistors, conductors, and prong engaging or prong holding conductive areas. The unit plate has a bottom edge recess in which a tube socket is seated, locked and held by its connectors being secured to such conductors. When the edge of the stage unit is seated on the face of the base plate the prongs and prong holding areas engage to make the electrical connections and provide some mechanical support. The socket has locking feet which project through an opening in the base plate and are engaged by a resilient removable locking ring to hold the unit in plugged-in place. Upon removal of the locking ring the stage unit may be disconnected from the base plate and another stage unit substituted. The prongs and prong holding areas easily connect and disconnect.

- Each stage unit may also include tubular capacitors mounted in apertures in the unit plate, and inductances mounted in slots in the edge of such unit plate. One solder dipping will suffice to attach the tubular capacitors, the tube socket and the inductances.

PLUG-IN CIRCUIT UNITS



June 23, 1960s J.N. Relay 2,882,130



Invention 2.0 : Miniature electronic circuits:

This invention relates to miniature electronic circuits, and more particularly to unique integrated electronic circuits fabricated from semiconductor material.

Many methods and techniques for miniaturising electronic circuits have been proposed in the past. At first, most of the effort was spent upon reducing the size of the components and packing them more closely together. Work directed toward reducing component size is still going on but has nearly reached a limit. Other efforts have been made to reduce the size of electronic circuits such as by eliminating the protective coverings from components, by using more or less conventional techniques to form components on a single substrate, and by providing the components with a uniform size and shape to permit closer spacings in the circuit packaging thereof.

All of these methods and techniques require a very large number and variety of operations in fabricating a complete circuit. For example, of all circuit components, resistors are usually considered the most simple to form, but when adapted for miniaturisation by conventional techniques, fabrication requires at least the following

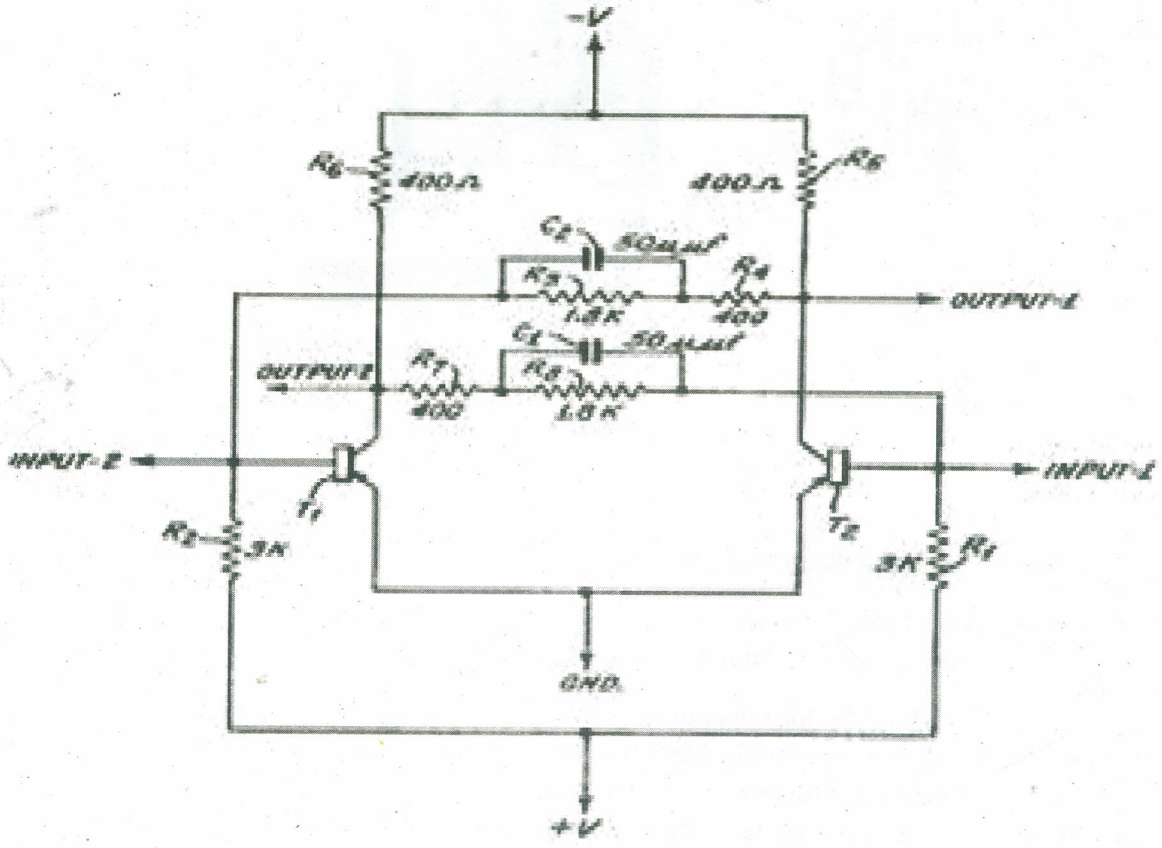
steps:

- Formation of the substrate
- Preparation of the substrate
- Application of terminations
- Preparation of resistor material.
- Application of the resistor material.
- Heat treatment of the resistor material.
- Protection or stabilisation of the resistor

June 23, 1964 J.S. KILBY 3,138,743

MINIAURIZED ELECTRONIC CIRCUIT

Filed Feb.06, 1959 4 Sheets-Sheat 3



INVENTOR
Jack S. Kilby

BY

Invention 3 : Method for making interconnects and diffusion barriers in *integrated circuits*

United States Patent Application : 20020094673
Date of Grant : July 18, 2002
Assignee: ***Intel* Corporation**
The inventor devised methods of forming interconnects that result in conductive structures with fewer voids and thus reduced electrical resistance. One embodiment of the method starts with an insulative layer having holes and trenches, fills the holes using a selective electroless deposition, and fills the trenches using a blanket deposition. Another embodiment of this method adds an anti-bonding material, such as a surfactant, to the metal before the electroless deposition, and removes at least some the surfactant after the deposition to form a gap between the deposited metal and interior sidewalls of the holes and trenches. The gap serves as a diffusion barrier. Another embodiments leaves the surfactant in place to serve as a diffusion barrier. These and other embodiments ultimately facilitate the speed, efficiency, or fabrication of integrated circuits.

Integrated circuits, the key components in thousands of electronic and computer products, are interconnected networks of electrical components fabricated on a common foundation, or substrate. Fabricators typically use various techniques, such as layering, doping, masking, and etching, to build thousands and even millions of microscopic resistors, transistors, and other electrical components on a silicon substrate, known as a wafer. The components are then wired, or interconnected, together to define a specific electric circuit, such as a computer processor.

To interconnect millions of microscopic components, fabricators sometimes use a dual-damascene metallisation technique, which takes its name from the ancient Damascan metalworking art of inlaying metal in grooves or channels to form ornamental patterns. The dual-damascene technique entails covering the components with an insulative layer, etching small holes in the insulative layer to expose portions of the components underneath, and etching shallow trenches from hole to hole to define a wiring pattern. Fabricators then execute a single deposition procedure, such as chemical or physical vapor deposition, to blanket the entire insulative layer with a thin sheet of aluminum. Some of this aluminium fills the holes and trenches and the rest lies on the higher surfaces of the insulative layer. The aluminum on these higher surfaces is then polished or scraped off, leaving behind aluminium vias, or contact plugs, in the holes and thin aluminum wires in the trenches. The wires are typically about one micron thick, or about 100 times thinner than a human hair.

This dual-damascene technique suffers from at least two problems. The first problem is that it uses a single-deposition procedure, which works fairly well for depositing aluminium into wide and shallow holes and trenches, but it is much less effective for narrow and deep ones, particularly those having width-to-depth, or aspect, ratios greater than five. For these aspect ratios, the single-deposition procedure using chemical or physical vapour deposition yields contact plugs and wires that have voids or cavities dispersed throughout and thus increased electrical resistance. Increased electrical resistance wastes power and slows down the transfer of electrical signals through an integrated circuit.

Fabricators have tried to solve this cavity problem, particularly for copper, using "reflow" techniques which entail depositing copper using standard cavity-prone methods and then heating the copper near its melting point. Melting the copper causes it to consolidate and thus eliminates cavities. However, these "reflow" techniques preclude the use of certain materials having melting points lower than that of the deposited metal. This is particularly true for some low-melting-point insulators which would improve integrated-circuit speed and efficiency.

The second problem with the conventional dual-damascene technique is its incompatibility with metals, such as gold, silver, and copper. These metals are more desirable than aluminium because their lower electrical resistance enhances efficiency and speed of integrated circuits and their higher electromigration resistance offers superior reliability. The incompatibility stems from how easy these metals diffuse through silicon-dioxide insulation and thus form short circuits with neighbouring wires. Although the diffusion can be prevented by cladding the contact plugs and wires in diffusion barriers, conventional dual-damascene techniques require extra deposition steps to form the barriers. These extra depositions are not only time-consuming but also increase the cost of fabrication.

Accordingly, there is a need for better methods of making contact plugs and wiring, especially methods of making high-aspect-ratio contact plugs and wiring from metals, such as gold, silver, and copper, and more efficient methods of making diffusion barriers.

SUMMARY OF THE INVENTION

To address these and other needs, the inventor devised a new dual-damascene method and a new method of making diffusion barriers for gold, silver, copper, and other metals. Specifically, one embodiment of the new dual-damascene method divides the single-deposition step of conventional dual-damascene techniques into two depositions: a selective electroless deposition for forming vias, or contact plugs with fewer voids, and a conventional deposition process, such as chemical or physical vapour deposition, to fill trenches. Other embodiments fill the trenches using an electroless deposition after forming barrier or seed layers in the trenches using chemical or physical vapour deposition.

One embodiment of the new method of making diffusion barriers entails adding a surfactant to a metal, depositing the metal on an insulative structure, and then removing at least some of the surfactant to form a gap, which serves as a diffusion barrier, between the deposited metal and the insulative structure. Another embodiment of this method leaves the surfactant in place to serve as a diffusion barrier.

Self Assessment Question **(Spend 3 minutes)**

3) Give examples of Integrated Circuits which come across in daily life electronic and digital equipments.

.....

.....

.....

.....

5.10 SUMMARY

- Semiconductor integrated circuits are at the heart of modern information, communications, entertainment, manufacturing, medical and space technologies, and are now finding their way into items as ordinary as house hold appliances.
- Today's integrated circuit products are constructed from a complex series of layers of Semiconductors, metals, insulators and other materials on a substrate. Intellectual Property Rights provides protection against copying of registered topographies, but does not prevent others from developing integrated circuit products which use other topographies to provide the same electronic functions.
- Some integrated circuit products, such as Random Access Memories (RAMS) and Read Only Memories (ROMS) may be used to store sets of instructions for electronic processors. In addition to the protection available for integrated circuit topographies embodied in such integrated circuits, the sets of instructions they store may be subject to protection under the Copyright Act as literary works and may in some cases be patentable as industrial methods.
- Other aspects of integrated circuit products may also be patentable, for example, the structure and method of operation of electronic circuits embodied in integrated circuit products, or industrial processes used to manufacture integrated circuit products. Indeed, protection available under the Patent Act can be much broader than the protection available under the Integrated Circuit Topography Act, and should therefore, be considered in addition to protection under the Integrated Circuit Topography Act.
- Protection in other countries should also be considered, particularly where significant market opportunities are expected, or where significant foreign competitors have manufacturing facilities.

5.11 TERMINAL QUESTIONS

1) What is a Integrated Circuit (IC) ? Give examples of IC.
2) Enumerate the key provisions for scope of Protection of IC as Intellectual Property Rights as per TRIPS.
3) Illustrate some of the key inventions in IC. Explain your understanding on what is protected as an Intellectual Property ?
4) Give reasons to illustrate the point - " Integrated Circuit can be protected as an Intellectual Property".
5) Write short notes on 1) Classification of IC 2) Fabrication of IC

5.12 ANSWERS AND HINTS

Self Assessment Questions

1) Read Section 1 to 6 and prepare a list of key learning points.
2) Read Section 7
3) Computers, mobile phone ..... etc.

Terminal Questions

1) Read Sections 5.1 & 5.2.
2) Read Section 5.7
3) Read Section 5.8
4) Read Section 5.7 & 5.8
5) Read Section 5.4 & 5.5

5.13 REFERENCES AND SUGGESTED READINGS

Baker, R. J. (2010). CMOS-*Circuit Design, Layout, and Simulation* - Third Edition. Wiley-IEEE. ISBN 978-0-470-88132-3.http://CMOSedu.com/

Hodges, D.A., Jackson H.G., and Saleh, R. (2003) - *Analysis and Design of Digital Integrated Circuits.*-McGraw-Hill. ISBN 0-07-228365-3.

Rabaey, J.M., Chandrakasan, A., and Nikolic, B. (2003) - *Digital Integrated Circuits*-2nd Edition. ISBN 0-13-090996-3

Mead, C. and Conway, L. (1980) - *Introduction to VLSI Systems.* Addison-Wesley. ISBN 0-201-04358-0.

UNIT 6 REGISTRATION OF LAYOUT-DESIGNS OF SEMICONDUCTOR ICs

Structure

6.1 Introduction

6.2 Objectives

6.3 Semiconductor Integrated Circuits Layout-Design (SICLD) Act, 2000

6.4 Salient Features of the Act

6.5 Criteria for Registration of a Chip Layout-Design

6.6 Rights Conferred on the Registered Proprietor of the Layout-Design

6.7 Duration of Registration

6.8 Powers of Registrar

6.9 Steps in the Registration of a Layout-Design

6.10 Registered User

6.11 Appellate Board Matters

6.12 Summary

6.13 Terminal Questions

6.14 Answers and Hints

6.15 References and Suggested Readings

6.1 INTRODUCTION

IC layout designs are important forms of Intellectual Property. Millions of dollars are invested by Corporations like Intel, Texas Instruments etc. to create niche Intellectual Property in the domain of Integrated Circuits. They are usually the result of an enormous investment, both in terms of the time of highly qualified experts, and financially. There is a continuing need for the creation of new layout-designs which reduce the dimensions of existing integrated circuits and simultaneously increase their functions. The smaller an integrated circuit, the less the material needed for its manufacture, and the smaller the space needed to accommodate it. Integrated circuits are utilised in a large range of products, including articles of everyday use, such as watches, television sets, washing machines, automobiles, etc., as well as sophisticated data processing equipment.

The possibility of copying by photographing each layer of an integrated circuit and preparing masks for its production on the basis of the photographs obtained is the main reason for the introduction of legislation for the protection of layout-designs.

In United States intellectual property law[1] (Semiconductor Chip Protection Act, 1984), a mask work is a two or three-dimensional layout or topography of an

[1] Integrated Circuit layout protection : http://en.wikipedia.org/wiki Integrated_circuit_layout_design_protection

integrated circuit (IC or "chip"), i.e. the arrangement on a chip of semiconductor devices such as transistors and passive electronic components such as resistors and interconnections. The layout is called a mask work because, in photolithographic processes, the multiple etched layers within actual ICs are each created using a mask, called the photo mask, to permit or block the light at specific locations, sometimes for hundreds of chips on a wafer simultaneously.

Because of the functional nature of the mask geometry, the designs cannot be effectively protected under copyright law (except perhaps as decorative art). Similarly, because individual lithographic mask works are not clearly protectable subject matter, they also cannot be effectively protected under patent law, although any processes implemented in the work may be patentable. So since the 1990s, national governments have been granting copyright-like intellectual property rights conferring time-limited exclusivity to reproduction of a particular layout.

A diplomatic conference was held at Washington, D.C., in 1989, which adopted a Treaty on Intellectual Property in Respect of Integrated Circuits (IPIC Treaty). The Treaty is open to States Members of WIPO or the United Nations and to intergovernmental organisations meeting certain criteria. The Treaty has been incorporated by reference into the TRIPS Agreement of the World Trade Organisation (WTO), subject to the following modifications: the term of protection is at least 10 (rather than eight) years from the date of filing an application or of the first commercial exploitation in the world, but Members may provide a term of protection of 15 years from the creation of the layout-design; the exclusive right of the right-holder extends also to articles incorporating integrated circuits in which a protected layout-design is incorporated, in so far as it continues to contain an unlawfully reproduced layout-design; the circumstances in which layout-designs may be used without the consent of right-holders are more restricted; certain acts engaged in unknowingly will not constitute infringement. TRIPS Articles

The Treaty on Intellectual Property in respect of Integrated Circuits, also called Washington Treaty or IPIC Treaty (signed at Washington on May 26, 1989) is not yet in force, having been ratified by only three countries, whereas five ratifications are needed to bring it into force. Hoiwever, major provisions of the treay have been integrated into the TRIPS agreement.

Article 35 of TRIPS in Relation to the IPIC Treaty states:

Members agree to provide protection to the layout-designs (topographies) of integrated circuits (referred to in this Agreement as "layout-designs") in accordance with Articles 2 through 7 (other than paragraph 3 of Article 6), Article 12 and paragraph 3 of Article 16 of the Treaty on Intellectual Property in Respect of Integrated Circuits and, in addition, to comply with the following provisions. TRIPS Document.

Article 2 of the IPIC Treaty gives the following definitions:

i) 'integrated circuit' means a product, in its final form or an intermediate form, in which the elements, at least one of which is an active element, and some or all of the inter-connections are integrally formed in and/or on a piece of material and which is intended to perform an electronic function,

ii) 'layout-design (topography)' means the three-dimensional disposition, however expressed, of the elements, at least one of which is an active element, and of some or all of the interconnections of an integrated circuit,

or such a three dimensional disposition prepared for an integrated circuit intended for manufacture ... "

Under the IPIC Treaty, each Contracting Party is obliged to secure, throughout its territory, intellectual property protection of layout-designs (topographies) of integrated circuits, whether or not the integrated circuit concerned is incorporated in an article. Such obligation applies to layout-designs that are original in the sense that they are the result of their creators' own intellectual effort and are not commonplace among creators of layout designs and manufacturers of integrated circuits at the time of their creation.

The Contracting Parties must, as a minimum, consider the following acts to be unlawful if performed without the authorisation of the holder of the right: the reproduction of the layout-design, and the importation, sale or other distribution for commercial purposes of the layout-design or an integrated circuit in which the layout-design is incorporated. However, certain acts may be freely performed for private purposes or for the sole purpose of evaluation, analysis, research or teaching.

The United States Code (USC) defines a mask work as "a series of related images, however fixed or encoded, having or representing the predetermined, three-dimensional pattern of metallic, insulating, or semiconductor material present or removed from the layers of a semiconductor chip product, and in which the relation of the images to one another is such that each image has the pattern of the surface of one form of the semiconductor chip product". Mask work exclusive rights were first granted in the US by the semiconductor Chip Protection Act of 1984.

According to 17 U.S.C. § 904, rights in Semiconductor mask works last 10 years. This contrasts with a term of 95 years for modern copyrighted works with a corporate authorship; alleged infringement of mask work rights are also not protected by a statutory fair use defense, nor by the typical backup copy exemptions that 17 U.S.C. § 117 provides for computer software. Nevertheless, as fair use in copyrighted works was originally recognised by the judiciary over a century before being codified in the Copyright Act of 1976, it's possible that the courts might likewise find a similar defense applies to mask work.

The exclusive rights in a mask work are somewhat like those of copyright: the right to reproduce the mask work or (initially) distribute an IC made using the mask work. Like the first sale doctrine, a lawful owner of an authorised IC containing a mask work may freely import, distribute or use, but not reproduce the chip (or the mask). Mask work protection is characterised as a *sui generis* right, i.e., one created to protect specific rights where other (more general) laws were inadequate or inappropriate.

Note that the exclusive rights granted to mask work owners are more limited than those granted to copyright or patent holders. For instance, modification (derivative works) is not an exclusive right of mask work owners. Similarly, the exclusive right of a patentee to "use" an invention would not prohibit an independently created mask work of identical geometry. Furthermore, reproduction for reverse engineering of a mask work is specifically permitted by the law. As with copyright, mask work rights exist when they are created, regardless of registration, unlike patents, which only confer rights after application, examination and issuance.

Mask work rights have more in common with copyrights than with other exclusive rights such as patents or trademarks. On the other hand, they are used alongside copyright to protect a read-only memory (ROM) component that is encoded to contain computer software.

The publisher of software for a cartridge-based video game console may seek simultaneous protection of its property under several legal constructs:

- a trademark registration on the game's title and possibly other marks such as fanciful names of worlds and characters used in the game (e.g., PAC-MAN®);
- a copyright registration on the programme as a literary work or on the audiovisual displays generated by the work; and
- a mask work registration on the ROM that contains the binary.

Salient features of the US Act

A sui generis law

Although the U.S. SCPA is codified in title 17 (copyrights), the SCPA is not a copyright or patent law. Rather, it is a sui generis law resembling a utility model law. It has some aspects of copyright law, some aspects of patent law, and in some ways it is completely different from either.

The Semiconductor Chip Protection Act of 1984 was an innovative solution to this new problem of technology-based industry. While some copyright principles underlie the law, as do some attributes of patent law, the Act was uniquely adapted to Semiconductor mask works, in order to achieve appropriate protection for original designs while meeting the competitive needs of the industry and serving the public interest.

In general, the chip topography laws of other nations are also sui generis laws. Nevertheless, copyright and patent case law illuminate many aspects of the SCPA and its interpretation.

Acquisition of protection by registration

Chip protection is acquired under the SCPA by filing with the U.S. Copyright Office an application for "mask work" registration under the SCPA, together with a filing fee. The application must be accompanied by identifying material, such as pictorial representations of the IC layers—so that, in the event of infringement litigation, it can be determined what the registration covers. Protection continues for ten years from the date of registration.

Mask works

The SCPA repeatedly refers to "mask works". This term is a relic of the original form of the bill that became the SCPA and was passed in the Senate as an amendment to the Copyright Act. The term mask work is parallel to and consistent with the terminology of the 1976 Copyright Act, which introduced the concept of "literary works", "pictorial works", "audiovisual works", and the like—and which protected physical embodiments of such works, such as books, paintings, video game cassettes, and the like against unauthorized

copying and distribution. This terminology became unnecessary when the House of Representatives insisted on the substitution of a sui generis bill, but the SCPA as enacted nonetheless continued its use. The term "mask work" is not limited to actual masks used in chip manufacture, but is defined broadly in the SCPA to include the topographic creation embodied in the masks and chips. Moreover, the SCPA protects any physical embodiment of a mask work.

Enforcement

The owner of mask work rights may pursue an alleged infringer ("chip pirate") by bringing an action for mask work infringement in federal district court. The remedies available correspond generally to those of copyright law and patent law.

Functionality unprotected

The SCPA does not protect functional aspects of chip designs. That is reserved to patent law. Although EPROM and other memory chips topographies are protectable under the SCPA, such protection does not extend to the information stored in chips, such as computer programs. Such information is protected, if at all, only by copyright law.

Reverse engineering not prohibited

The SCPA permits competitive emulation of a chip by means of reverse engineering. The ordinary test for illegal copying (mask work infringement) is the "substantial similarity" test of copyright law, but when the defense of reverse engineering is involved and supported by probative evidence (usually, the so-called paper trail of design and development work), the similarity must be greater. Then, the accused chip topography must be substantially identical (truly copied by rote, so-called slavish copying), rather than just substantially similar, for the defendant to be liable for infringement. Most world chip topography protection laws provide for a reverse engineering privilege.

Self Assessment Questions **(Spend 2 minutes)**

1) Identify and understand what is the Intellectual Property that covers IC Circuits.

.....

.....

.....

.....

2) What is the limitations which has prompted for a separate act on IC Circuit Protection?

.....

.....

.....

6.2 OBJECTIVES

After reading this unit, you should be able to:

- illustrate the intellectual property rights on entegrated circuits;
- enumerate the sacient feature of the Indian (SICLD, Semiconductor integrated circuit layout Design Act, 2000); and
- explain the protection of Semiconductor integrated circuits and layout design in India.

6.3 SEMICONDUCTOR INTEGRATED CIRCUITS LAYOUT-DESIGN (SICLD) ACT, 2000

It provides for the protection of semiconductor integrated circuits layout-designs and for matters connected therewith or incidental thereto. According to the Act, the term 'layout-design' means "a layout of transistors and other circuitry elements and includes lead wires connecting such elements and expressed in any manner in a Semiconductor integrated circuit". Here, the term 'semiconductor integrated circuit' means "a product having transistors and other circuitry elements which are inseparably formed on a semiconductor material or an insulating material or inside the Semiconductor material and designed to perform an electronic circuitry function".

The Act is implemented by the **Department of Electronics and Information Technology**, Ministry of Communications and Information Technology. The Act is applicable to Integrated Circuits Layout-Design IPR applications filed at the Registry in India. The **Semiconductor Integrated Circuits Layout-Design Registry (SICLDR)** is the office where the applications on Layout-Designs of integrated circuits are filed for registration of created IPR. The Registry has jurisdiction all over India.

6.4 SALIENT FEATURES OF THE ACT

The aim of the Semiconductor Integrated Circuits Layout-Design Act, 2000 is to provide protection of Intellectual Property Right (IPR) in the area of Semiconductor Integrated Circuit Layout Designs and for matters connected therewith or incidental thereto.

The SICLD Act 2000 was gazetted on the 4th September 2000 (Part II-Section I, No. 46). The rules under the Act have been gazetted on December 11, 2001 (Part II. Section 3, No 615). The Act is being implemented in stages. Sections 3 and 5 of the Act have been brought to force w.e.f. 1.5.2004.

SICLD Act is a sui-generis (one of its kind)law specifically meant for protecting IPR relating to Layout-Design (Topographies) of Semiconductor Integrated Circuit.

- For the purposes of this Act, a record called the 'Register of Layout-Designs' shall be kept at the head office of the Semiconductor Integrated Circuits Layout-Design Registry, wherein shall be entered all registered layout-designs with the names, addresses and descriptions of the proprietor and such other matters related to the registered layout-designs as may be prescribed.

MIP-103-2-52-1000

- Prohibition of registration of those layout-designs which:-
  - Are not original; or
  - Have been commercially exploited anywhere in India or in a convention country; or
  - Are not inherently distinctive; or
  - Are not inherently capable of being distinguishable from any other registered layout-design.
- A layout-design shall be considered to be original if it is the result of its creator's own intellectual efforts and is not commonly known to the creators of layout-designs and manufacturers of Semiconductor integrated circuits at the time of its creation. Any person claiming to be the creator of a layout-design, who is desirous of registering it, shall apply in writing to the Registrar in the prescribed manner for the registration of his layout-design. Every application shall be filed in the office of the Semiconductor Integrated Circuits Layout-Design Registry within whose territorial limits; the principal place of business of the applicant is situated in India.

Key Definitions

Semiconductor Integrated Circuit means a product having transistors and other circuitry elements, which are inseparably formed on a Semiconductor material or an insulating material or inside the Semiconductor material and designed to perform an electronic circuitry function.

The layout-design of a Semiconductor integrated circuit means a layout of transistors and other circuitry elements and includes lead wires connecting such elements and expressed in any manner in Semiconductor integrated circuits.

The Central Government may, by notification in the Official Gazette, appoint a person to be known as the 'Registrar of Semiconductor Integrated Circuits Layout-Design' for the purposes of this Act. Also, there shall be a 'Semiconductor Integrated Circuits Layout-Design Registry' for the purposes of facilitating the registration of layout-designs at such places as the Central Government may specify.

- When an application for registration of a layout-design has been accepted, the Registrar shall, within fourteen days after the date of acceptance, cause the application as accepted to be advertised in the prescribed manner.
- Any person may, within three months from the date of the advertisement or re-advertisement of an application for registration or within such further period, not exceeding one month in the aggregate give notice in writing in the prescribed manner to the Registrar, of opposition to the registration. The Registrar shall serve a copy of the notice on the applicant for registration and, within two months from the receipt by the applicant of such copy of the notice of opposition, the applicant shall send to the Registrar in the prescribed manner

a counter-statement of the grounds on which he relies for his application and if he does not do so, he shall be deemed to have abandoned his application.

- Also, where registration of a layout-design is not completed within twelve months from the date of the application by reason of default on the part of the applicant, the Registrar may, after giving notice to the applicant in the prescribed manner, treat the application as abandoned unless it is completed within the time specified in that behalf in the notice.
- The registration of a layout-design shall be only for a period of ten years counted from the date of filing an application for registration or from the date of first commercial exploitation anywhere in India or in any country, whichever is earlier.
- A registered layout-design is infringed by a person who, not being the registered proprietor of the layout-design or a registered user thereof:-
  - Does any act of reproducing, whether by incorporating in a Semiconductor integrated circuit or otherwise, a registered layout-design in its entirety or any part thereof, which is not original within the meaning of the Act.
  - Does any act of importing or selling or otherwise distributing for commercial purposes a registered layout-design or a Semiconductor integrated circuit, incorporating such registered layout-design or an article incorporating such a Semiconductor integrated circuit, containing such registered layout-design for the use of which such person is not entitled under the Act?
- Any person who contravenes knowingly and wilfully any of the provisions of the Act or falsely represent a layout-design as registered, shall be punishable with imprisonment or with fine or with both

Major Provisions of the Act

Jurisdiction to the whole of India

- SICLD Registry as the front end - where the layout-designs of integrated circuit chips can be registered
- Defines layout-designs of integrated circuits which can be registered under the Act
- Defines duration of registration of layout-designs
- Defines rights conferred by registration
- Defines matters of infringement of layout-designs
- Defines procedures for assignment and transmission of registered layout-design
- Provides for registered users for using registered layout-design
- Provides for an Appellate Board as a forum of redressal
- Provides for provisions in matter of national emergency or extreme public urgency

- Specifies penalty in case of :
  - infringement of layout-design
  - falsely representing a layout-design as registered
  - improperly describing a place of business
  - falsification of entries in the register
  - forfeiture of goods
  - offences by companies
- Provision for agents
- Reciprocity provision with other recognised countries

Self Assessment Question **(Spend 2 minutes)**

3) List down your key learning Points on IC Circuit as an Intellectual Property as per the SICLD Act, 2000.

.....

.....

.....

.....

.....

.....

.....

6.5 CRITERIA FOR REGISTRATION OF A CHIP LAYOUT-DESIGN

A Layout design that is:

- Original
- Not commercially exploited anywhere in India or convention /reciprocal country
- Inherently distinctive
- Inherently capable of being capable of being distinguishable from any other registered layout design.
- Capable of being registered.

"Only the Layout-Design" – which essentially is the mask layout – floor planning of the integrated circuits can be registered under the SICLD Act 2000 and not the other information like any idea, procedure, process, system, programme stored in the integrated circuit, method of operation etc.

6.6 RIGHTS CONFERRED ON THE REGISTERED PROPRIETOR OF THE LAYOUT-DESIGN

The SICLD Act empowers the registered proprietor of the layout-design an inherent right to use the layout-design, commercially exploit it and obtain relief in respect of any infringement. *The Act allows two or more persons as joint proprietors of a layout-design*[2].

This Act is applicable for IC Layout-Design IPR applications filed at the Registry in India .The main focus of SICLD Act is to provide for routes and mechanism for protection of IPR in Chip Layout Designs created and matters related to it.

Semiconductor Integrated Circuits Layout-Design Registry (SICLDR) is the office where the applications on Layout-Designs of integrated circuits are filed for registration of created IPR . This Registry is located at Room no. 3014-3015, Electronics Niketan, Department of Information Technology, 6 CGO Complex, Lodi Road, New Delhi-110 003.

Commercial Exploitation

Only the layout-designs created by the creators through own intellectual efforts and commonly not known to the creators at the time of creation; or inherently distinctive from other registered layout-designs or have not been commercially exploited in India; or a convention country for more than two (2) years can be registered under the Act[3].

Commercial exploitation implies acts such as sell, lease, offer or exhibit for sale or otherwise distribute such Semiconductor integrated circuit for commercial purpose.

6.7 DURATION OF REGISTRATION

A period of 10 years counted from the date of filing an application for registration or from the date of first commercial exploitation anywhere in India or in any convention country or country specified by Government of India whichever is earlier.

Who can obtain protection of Layout – Designs under the SICLD Act 2000 ?

Any person(s) who:

is creator of a layout design and desires to register it

is an Indian national or national of country outside India which accords to citizens of India similar privileges as granted to its own citizens in respect of registration and protection of layout-designs and

has principal place of business in India or if he does not carry out business in India, has place of service in India.

[2] Section 14 of the Act.

[3] Section 7 of the Act.

6.8 POWERS OF REGISTRAR

Section 72 of the Act be referred for full details. Major ones are:

- All powers of a civil court for the purposes of
  - receiving evidence, administering oaths, enforcing the attendance of witnesses compelling the discovery and production of documents and
  - issuing commissions for examination the of witnesses.
- The Registrar may make orders under Section 96 of the Act as to costs he considers reasonable and any such order shall be executable as decree to a civil court
- Examine applications filed and issue registration to the qualifying layout designs
- Supervise and approve all administrative and technical actions in matters of Registry
- Refer disputes to the Appellate Board
- Review his own decisions
- May cancel the registration of registered user

The Registrar will determine the originality of the design based on the information available with him as also through the mechanism of advertisement of the application for registration of the layout-design and or any input he may receive.

The Registrar will issue the certificate of registration with the seal of Semiconductor Integrated Circuits Layout-Design Registry

6.9 STEPS IN REGISTRATION OF A LAYOUT-DESIGN

The registration of a layout-design involves the following steps:

- Filing of application by the creator of the layout-design at the SICLD Registry.
- The acceptance of application. Registrar may accept, refuse the application or accept with some modifications.
- The accepted applications shall be advertised within 14 days of acceptance.
- Any opposition to the advertisement can be filed within 3 months from the date of advertisement.
- The counter-statement to the notice of opposition, if any, to be filed within 2 months from the date of receipt of copy of notice of opposition from the Registrar.
- A copy of the counter statement provided to the opposing party.
- The Registrar may take hearing with the parities.

- The Registrar will decide on the originality of the layout-design and grant or reject the application for registration based on the conclusions reached by him.
- Aggrieved party can appeal to Appellate Board or in its absence Civil Court for relief on any ruling of the Registrar.

Documents /material to be given at the Registry at the time of filing IPR application

Registrar's office has drawn a list of items to be submitted along with the application. This is available at the Registrar's office. The list includes:

i) three sets of 2D/3D drawings which describe the layout-design applied for registration and or 3 sets of photographs of masks used for the fabrication of the Semiconductor integrated circuit by using of the layout-design applied for registration, and or drawings which describe the pattern of such masks

ii) Semiconductor integrated circuit [where an integrated circuit has been made using layout-design applied for registration]

iii) any related information sought by Registry/Registrar.

Self Assessment Question **(Spend 2 minutes)**

4) List out the important steps to be followed for registration of IC.

.....

.....

.....

.....

Register of Layout-Designs

Register of Layout-Designs is a register wherein all registered layout-designs with names, addresses and descriptions of the proprietor and other matters related to the registered layout-designs are listed in a central Register maintained at the Registry. This Register is open to public on payment of charges.

The Registrar and/or Layout-Design Appellate Board can rectify the Register of Layout-Designs. In addition to this, Registrar can make the following corrections in the Register:

a) correct any error in the name, address or description of the registered proprietor of a layout-design, or any other entry relating to the layout-design

b) enter any change in the name, address or description of the person who is registered as proprietor of a layout-design

c) cancel the entry of a layout-design on the register

d) correct any errors in entries.

The public can inspect the following documents on payment of related fees:

a) the Register of layout-designs and any document upon which any entry in the register is based

b) notice of opposition to the registration of a layout-design application for rectification before the Registrar, counter statement thereto, and any affidavit or document filed by the parties in any proceedings before the Registrar

c) the indexes (as indicated in Section 86 of the Act).

6.10 REGISTERED USER

Persons,other thanthe registered proprietor, who want to use the layout-design may get themselves registered as registered users. The application for registration as a user is to be filed jointly by the registered proprietor and the proposed user. Such application should be accompanied by the following:

a) The agreement in writing or a duly authenticated copy thereof, entered into between the registered proprietor and the proposed registered user with respect to the permitted use of the layout-design; and

b) An affidavit made by the registered proprietor or by some person authorised to the satisfaction of Registrar to act on his behalf-

   i) Giving particulars of the relationship, existing or proposed, between the registered proprietor and the proposed registered user, including particulars showing the degree of control by the proprietor over the permitted use which the relationship will confer and whether it is a term of their relationship that the proposed registered user shall be sole registered user or that there shall be any other restriction as to persons for whose registration as registered user application may be made;

   ii) Stating the conditions or restrictions, if any, proposed with respect to the place of permitted use or any other matter;

   iii) Stating whether the permitted use to be for a period or without limit of period, and, if for a period, the duration thereof; and.

c) such further documents or other evidence as may be required by the Registrar or as may be prescribed.

The Registrar can cancel the registration of a registered user on any of the following grounds:

i) That the registered user has used the layout-design otherwise than in accordance with the agreement under clause (a) of Sub-section (1) of Section 25;

ii) That the proprietor or the registered user misrepresented, or failed to disclose, some fact material to the application for registration which if accurately represented or disclosed would not have justified the registration of the registered user;

iii) That the circumstances have changed since the date of registration in such a way that at the date of such application for cancellation they would not have justified registration of the registered user;

iv) That the registration ought not to have been effected having regard to right vested in the applicant by virtue of a contract in the performance of which he is interested.

The registration may also be cancelled by the Registrar on his own motion or on the application in writing in the prescribed manner by any person on the ground that any stipulation in the agreement between the registered proprietor and the registered user regarding the too graphical dimensions of the layout-design is either not being enforced or is not being complied with.

Another ground for cancellation is that the layout-design is nolonger registered.

The Act does not confer on a registered user of a layout-design any assignable or transmissible right to use thereof.

6.11 APPELLATE BOARD MATTERS

Layout-Design Appellate Board (LDAB) or in its absence the Intellectual Property Appellate Board (IPAB) constituted under Trademarks Act, 1999 will be the Appellate forum. IPAB is located in Chennai.

The following are the broad functions of the Appellate Board:

- Rectify the Register of Layout-Designs
- Determine Royalty in case of use of the registered layout-design by a user who had no prior knowledge that the layout-design was registered i.e. innocent infringement
- Cancel registration of a layout-design (as per Section 41 of the Act)
- Listen to the appeals made against the decisions of the Registrar and decide appropriately
- Decide the cases referred to by the Registrar
- Permit use of registered layout-design without the authorisation of the registered proprietor (as per Section 51 of the Act). Appellate Board will have the same powers as vested in a civil court under the Code of Civil Procedure, 108 while trying a suit in respect of the following matters
    - receiving evidence
    - issuing commissions for examination of witnesses
    - requisitioning any public record etc.

The Act provides for the Layout-Design Appellate Board to authorise the Government or any person authorised by the Government, after giving notice to the registered proprietor of the layout-design, permit use of the registered layout-design, for a limited period subject to the following conditions (Section 51 of the Act):

- the use shall be for non-commercial public purposes or purposes related to national emergency or of extreme public urgency
- the use is to remedy the anti-competitive practices
- the use is non-assignable and non-transmissible
- the use is for supplying ICs or articles incorporating these ICs for domestic market of India only

MIP-103-2-52-1000

While granting a compulsory license the Appellate Board can determine the amount to be paid as royalty by the Government or the person authorised by the Government, as the case may be, to the registered proprietor of the layout-design.

The registered proprietor of the layout-design can appeal the Appellate Board to review the compulsory license granted under Section 51 of the Act. The Board can amend or cancel such permission if it is satisfied that any of the conditions subject to which the permission was earlier granted has not been observed or the circumstances, which led to the granting of such permission, has ceased to exist or substantially altered.

Appeal in the High Court can be made against order of the Appellate Board. Infringing the rights of a registered proprietor of a layout-design is a considered a criminal offence. The infringer is punishable with imprisonment for a term that may extend to three (3) years or fine which shall not be less than Rs. 50,000/- but which may extend to Rs. 10.0 lakhs or with both.

It is a criminal offence to falsely represent a layout-design as registered. If a person does so, he can be punished with imprisonment for a term that may extend to 6 months or with fine, which may extend to Rs. 50,000/- or with both.

It is a criminal offence to improperly describe a place of business as connected with SICLD Registry. If a person does so, he can be punished with imprisonment for a term that may extend to 6 months or with fine or with both.

Falsification of entries in the register is a criminal offence. If a person does so, he can be punished with imprisonment for a term that may extend to two (2) years or with fine or with both.

The entitlement to institute any proceeding to prevent, or to recover damages for the infringement of an unregistered layout-design.

A person can approach registration of his layout-design under the Act provided he is able to satisfy that his work is original and created through his own intellectual efforts and meets criteria of registerability as per Section 7. Any innocent action is entitled to immunity from infringement.

The Registrar can extend time for doing any act, whether the time so specified has expired or not, subject to such conditions as he may think fit to impose. However, no relaxation in the time limit of commercial exploitation i.e. two years is possible.

The following duly authorised persons, instead of the person himself, can do any act other than making of an affidavit on the behalf of such person:

- legal practitioner
- person registered as layout-design agent in the Registry
- person in the sole and regular employment of the principal.

6.12 SUMMARY

- Because of the functional nature of the Integrated Circuits layouts and the mask geometry, the designs cannot be effectively protected under copyright law. Further, individual lithographic mask works are not clearly protectable

subject matter; they also cannot be effectively protected under patent law, although any processes implemented in the work may be patentable. This led to the enactment of Semiconductor Integrated Circuits Layout-Design (SICLD) Act, 2000 by Govt. of India.

- The above act provides for the protection of Semiconductor integrated circuits layout-designs. The Act, defines the term 'layout-design' as "a layout of transistors and other circuitry elements and includes lead wires connecting such elements and expressed in any manner in a Semiconductor integrated circuit". Here, the term 'Semiconductor integrated circuit' means "a product having transistors and other circuitry elements which are inseparably formed on a Semiconductor material or an insulating material or inside the Semiconductor material and designed to perform an electronic circuitry function".
- At the International level, diplomatic conference was held at Washington, D.C., in 1989, which adopted a treaty on Intellectual Property in Respect of Integrated Circuits (IPIC Treaty). The Treaty paved way for States Members of WIPO or the United Nations to have a framework for national legislations for protection of layout designs. The Treaty has been formulated with close reference to TRIPS Agreement of the World Trade Organisation (WTO), with slight modifications. The term of protection is at least 10 years from the date of filing an application or of the first commercial exploitation in the world, but Members may provide a term of protection of 15 years from the creation of the layout-design.
- As per SICLD Act 2000- a period of 10 years is counted from the date of filing an application for registration or from the date of first commercial exploitation anywhere in India or in any convention country or country specified by Government of India whichever is earlier.

6.13 TERMINAL QUESTIONS

1) What is the definition of the Semiconductor Integrated Circuit as per the SICLD Act, 2000?
2) Enumerate the criteria for protection of chip lay out design.
3) Illustrate the key steps to be followed for registration of layout design as per the SICLD Act, 2000.
4) Give reasons to illustrate the limitations of protections of IC through Patents and Copyrights.
5) Write short notes on 1) Layout-Design Appellate Board (LDAB) Cancellation of registration of Layout Design.

6.14 ANSWERS AND HINTS

Self Assessment Questions

1) It is not a Process or Product nor a Copyrightable matter ....
2) Read Section 6.2
3) Read Section 6,4
4) Read Section 6.9

Terminal Questions

1) Read Section 6.4
2) Read Section 6.5
3) Read Section 6.9
4) Read Section 6.2
5) Read Section 6.9

6.15 REFERENCES AND SUGGESTED READINGS

Richard H. Stern, *Semiconductor Chip Protection, Harcourt Brace/Aspen Law & Business* (June 1985), ISBN 978-0317294136.

Symposium: *The Semiconductor Chip Protection Act of 1984 and Its Lessons, 70 Minn. L. Rev. 263 (1985)* six law review articles on SCPA.

The first chip-layout copying case, IEEE Micro, v. 11, no. 4. Aug 1991. Also available at this link. Technical article on proof of chip copying.

Baker, R. J. (2010): *CMOS-Circuit Design, Layout, and Simulation -Third Edition.* Wiley-IEEE. ISBN 978-0-470-88132-3

Hodges, D.A., Jackson H.G., and Saleh, R. (2003): *Analysis and Design of Digital Integrated Circuits.*-McGraw-Hill. ISBN 0-07-228365-3.

Rabaey, J.M., Chandrakasan, A., and Nikolic, B. (2003): *Digital Integrated Circuits-2nd Edition.* ISBN 0-13-090996-3

Mead, C. and Conway, L. (1980): *Introduction to VLSI Systems.* Addison-Wesley. ISBN 0-201-04358-0.

UNIT 7 RIGHTS ACQUIRED BY REGISTRATION OF INTEGRATED CIRCUITS

Structure

7.1 Introduction

7.2 Objectives

7.3 Registration

7.4 Rights Conferred by Registration

7.5 Infringement of Layout-Design

7.6 Criteria for Infringement and Non-infringement as per the SICLD Act, 2000

7.7 Registration and Prima Facie Evidence of Validity

7.8 Assignment and Transmission

7.9 Case Study to Explain the Concept of Infringement

7.10 Summary

7.11 Terminal Questions

7.12 Answers and Hints

7.13 References and Suggested Readings

7.1 INTRODUCTION

In the semiconductor industry, innovation is indispensable; research breakthroughs are essential to the life and health of the industry. But research and innovation in the design of semiconductor chips are threatened by the inadequacies of existing legal protection against piracy and unauthorised copying.

The semiconductor chip was invented in 1959; and the first microprocessor chip was developed in 1971. By the early 1980s, developers could fabricate chips containing more than 100,000 transistors. From the 1970s through to the 1990s, the chip has become so ubiquitous that it is found in products ranging from automobiles to refrigerators to personal computers and a vast variety of "personal electronics".

Since the early 1980s, the pace of innovation in semiconductor technology has accelerated. Chips currently in production contain in excess of 1,000,000 transistors. Dynamic random access memory chips (DRAMS), which have set the pace of progress in the industry, have provided a fourfold increase in capacity *every three years* — even though each increase has required engineers and scientists to solve ever more complex problems, driving the technology to even greater heights.

The photolithographic process used to fabricate the vast majority of semiconductor chips is conceptually relatively simple. The manufacturer applies a layer of photoresist (a material that reacts to light and resists the action of certain chemical

agents) to a wafer of material called a substrate. The photoresist is exposed with a predetermined pattern. After being "developed", portions of the photoresist are washed away, leaving the substrate exposed. The substrate is then treated with a chemical agent that may etch material away from the exposed part, deposit material on it, or permeate into it. The manufacturer removes the photoresist and then repeats the process for each of the multiple layers required to form the device.

The photolithographic process just described has many applications beyond semiconductor chips. The substrate does not have to be silicon (or any semiconductor for that matter), and the product does not have to be electronic circuitry. Manufacturers can use photolithography with masks on a variety of substrate materials, such as glass, polycrystalline silicon, sapphire, ceramic material, superconducting material, magnetic domain material — the list goes on and on, and continues to grow.

Moreover, the resulting product does not have to be a "chip." It can be a flat-panel display, a miniature motor and gears, a thin-film recording head, or any one of a number of items that are not usually considered to be electronic circuitry. It is possible that within a few years, virtually every portion of computer hardware, from the display to the mass storage devices to the packaging for chips will be fabricated by using some kind of masking process.

Each stage of the process, from preliminary design through fabrication, requires investment, skill, creativity, and just plain hard work. As the technology became increasingly important in, additional legal protection at some stage of the process appeared to be necessary to protect this investment if innovation was to flourish.

7.2 OBJECTIVES

After reading this unit, you should be able to:

- explain the nature of right acquired by regulation of IC layout as part the (SICLD) Act, 2000; and
- discuss the infringement of rights with example.

7.3 REGISTRATION

- Subject to the provisions of Section 9 of the Semiconductor Integrated Circuits Layout-Design Act, 2000, when an application for the registration of the layout-design has been accepted and either-

  a) The application has not been opposed and time for notice of opposition has expired; or

  b) The application has been opposed and the opposition has been decided in favour of the applicant,

  The Registrar shall register the said layout-design in the register and the layout-design shall be registered as of the date of the making of the said application and that date shall be deemed to be the date of registration.

- On the registration of a layout-design, the Registrar shall issue to the applicant a certificate in the prescribed form of the registration thereof sealed with the seal of the Semiconductor Integrated Circuits Layout-Design Registry.

- Where registration of a layout-design is not completed within twelve months from the date of the application by reason of default on the part of the applicant, the Registrar may, after giving notice to the applicant in the prescribed manner, treat the application as abandoned unless it is completed within the time specified in that behalf in the notice.

The registration of a layout-design shall be only for a period of ten years counted from the date of filing an application for registration or from the date of first commercial exploitation anywhere in India or in any country whichever is earlier. No action of infringement of unregistered layout-design and No person shall be entitled to institute any proceeding to prevent, or to recover damages for, the infringement of an unregistered layout-design.

Self Assessment Question **(Spend 2 minutes)**

1) List down the provisions of the *Semiconductor Integrated Circuits Layout-Design Act, 2000* act which confers registration.

.....

.....

.....

.....

. .....

7.4 RIGHTS CONFERRED BY REGISTRATION

The registration of a layout design shall give to the registered proprietor of layout design the exclusive right to the use of the layout-design and to obtain relief in respect of infringement in the manner provided by this Act. The rights conferred by the registration of a layout-design shall be available to the registered proprietor of that layout-design irrespective of the fact as to whether the layout-design is incorporated in an article or not.

7.5 INFRINGEMENT OF LAYOUT-DESIGN

A registered layout-design is infringed by a person who, not being the registered proprietor of the layout-design or a registered user thereof,-

- Does any act of reproducing, whether by incorporating in a semiconductor integrated circuit or otherwise, a registered layout-design in its entirety or any part thereof, except such act of reproducing any part thereof which is not original[1] .
- Does any act of importing or selling or otherwise distributing for commercial purposes[2] a registered layout-design or a semiconductor integrated circuit incorporating such registered layout-design or an article incorporating such

[1] within the meaning of sub-section (2) of Section 7;

[2] subject to the provisions of Sub-section (5),

a semiconductor integrated circuit containing such registered layout-design for the use of which such person is not entitled under this Act.

7.6 CRITERIA FOR INFRINGEMENT AND NON-INFRINGEMENT AS PER SICLD ACT, 2000

Notwithstanding anything contained in Section 17, Sub-section (1) or Sub-section (5), the performance of the act of reproduction referred to in clause (a) of Sub-section (1), where such act is performed for the limited purposes of scientific evaluation, analysis, research or teaching, shall not constitute act of infringement within the meaning of that clause.

Where a person, on the basis of scientific evaluation or analysis of a registered layout-design, creates another layout-design which is original within the meaning of Sub-section (2) of Section 7, that person shall have the right to incorporate such another layout-design in a semiconductor integrated circuit or to perform any of the acts referred to in Sub-section (1) or Sub-section (5) in respect of such another layout-design and such incorporation or performance of any act shall not be regarded as infringement within the meaning of Sub-section (1).

Where a layout-design is created by the process of scientific evaluation or analysis of the registered layout-design as referred to in Sub-section (3), the use of such layout-design by the proprietor of such registered layout-design shall be regarded as infringement within the meaning of Sub-section (1) after the date of registration of such layout-design under this Act.

Notwithstanding anything contained in clause (b) of Sub-section (1), the performance of any of the acts referred to in that clause by a person shall not be regarded as infringement within the meaning of that clause if such act is performed or directed to be performed in respect of a semiconductor integrated circuit incorporating a registered layout-design or any article incorporating such a semiconductor integrated circuit where such person does not possess any knowledge or has no reasonable ground to know while performing or directing to be performed such act in respect of such semiconductor integrated circuit or article that it incorporated a registered layout-design but after the time when such person has received notice of such knowledge, he may continue to perform or directing to be performed such act in respect of the stock on hand or ordered before such time and, then, he shall be liable to pay the proprietor of the registered layout-design a sum by way of royalty to be determined by negotiation between registered proprietor of the registered layout-design and that person or by the Appellate Board having regard to the benefit accrued to such person by performing or directing to be performed such act in respect of such semiconductor integrated circuit or article, as the case may be.

Where any other person purchases a semiconductor integrated circuit incorporating a registered layout-design or any article incorporating such a semiconductor integrated circuit referred to in Sub-section (5)

from a person referred to in that Sub-section, then, such other person shall be entitled to the immunity from infringement in respect of that semiconductor integrated circuit or article, as the case may be, to the extent and in the manner as if the word "person" referred in that sub-section includes the word any other person referred in this sub-section.

Nothing contained in clause (b) of Sub-section (1) shall be construed as constituting an act of infringement where any person performs any of the acts specified in that clause with the written consent of the registered proprietor of a registered layout-design or within the control of the person obtaining such consent, or in respect of a registered layout-design or a semiconductor integrated circuit incorporating a registered layout-design or any article incorporating such a semiconductor integrated circuit, that has been put on the market by or with the consent of the registered proprietor of such registered layout-design.

Notwithstanding anything contained in this Act, where any person by application of independent intellect has created a layout-design which is identical to a registered layout-design, then, any act of such person in respect of the layout-design so created shall not be the infringement of the registered layout-design.

Self Assessment Questions **(Spend 2 minutes)**

2) What are the basic rights conferred upon registration.

.....

.....

.....

.....

3) Understand the concept of Infringement as per the provisions of the Semiconductor Integrated Circuits Layout-Design Act, 2000.

.....

.....

.....

.....

7.7 REGISTRATION AND PRIMA FACIE EVIDENCE OF VALIDITY

- In all legal proceedings relating to a layout-design registered under this Act (including application under Section 30), the original registration of the layout-design and all Subsequent assignments and transmissions of layout-design shall be *prima facie* evidence of the validity thereof.

- In all legal proceedings as aforesaid, a registered layout-design shall not be held to be invalid on the ground that it was not a register able layout-design[3] except upon evidence of originality and that such evidence was not submitted to the Registrar before registration.

7.8 ASSIGNMENT AND TRANSMISSION

- The person for the time being included in the register as proprietor of a layout-design shall, subject to any right appearing from the register to be vested in any other person, have power to assign the layout-design, and to give effectual receipts for any consideration for such assignment.
- Notwithstanding anything in any other law to the contrary, a registered layout-design shall be assignable and transmissible whether with or without the goodwill of the business concerned.
- Where an assignment of a registered layout-design is made otherwise than in connection with the goodwill of business in which such layout-design has been or is used, the assignment shall not take effect unless the assignee, not later than the expiration of six months from the date on which the assignment is made or within such extended period, if any, not exceeding three months in the aggregate, as the Registrar may allow, apply to the Registrar for directions with respect to the advertisement of the assignment, and advertises it in such form and manner and within such period as the Registrar may direct.
- Where a person becomes entitled by assignment or transmission to a registered layout-design, he shall apply in the prescribed manner to the Registrar to register his title, and the Registrar shall, on receipt of the application and on proof of his title to his satisfaction, register him as the proprietor of the layout-design and shall cause particulars of the assignment or transmission to be entered on the register: Provided that where the validity of an assignment or transmission is in dispute between the parties, the Registrar may refuse to register the assignment or transmission until the rights of the party have been determined by a competent court.
- Except for the purpose of an application before the Registrar under Sub-section (1) or an appeal from an order thereon, or an application under Section 30 or an appeal from an order thereon, a document or instrument in respect of which no entry has been made in the register in accordance with Sub-section (1), shall not be admitted in evidence by the Registrar or the Appellate Board or any court in proof of title to the layout-design by assignment or transmission unless the Registrar or the Appellate Board or the court, as the case may be, otherwise directs.

7.9 CASE STUDY TO EXPLAIN THE CONCEPT OF INFRINGEMENT

In the United States of America, the Semiconductor Chip Protection Act of 1984 prohibits "chip piracy"— the unauthorised copying and distribution of semiconductor chip products copied from the original creators of such works.

[3] under section 7.

In the evolution of the Semiconductor Chip Protection Act it was first proposed simply to amend the Copyright Act[4], to include semiconductor chip products and mask works as subject of copyright.

However, although some courts had interpreted copyright law as applicable to computer software imbedded in a semiconductor chip, see Apple Computer, Inc. v. Franklin Computer Corp[5]., it was uncertain whether the copyright law could protect against copying of the pattern on the chip itself, if the pattern was deemed inseparable from the utilitarian function of the chip. Indeed, the Copyright Office had refused to register patterns on printed circuit boards and semiconductor chips because no separate artistic aspects had been demonstrated.

Concern was also expressed that extension of the copyright law to accommodate the problems of mask works would distort certain settled copyright doctrines, such as fair use.

The patent system alone was deemed not to provide the desired scope of protection of mask works. Although electronic circuitry and electronic components are within the statutory subject matter of patentable invention and some original circuitry may be patentable if it also meets the requirements of the Patent Act, as is illustrated in this case, Congress sought more expeditious protection against copying of original circuit layouts, whether or not they met the criteria of patentable invention.

The Semiconductor Chip Protection Act of 1984 was an innovative solution to this new problem of technology-based industry. While some copyright principles underlie the law, as do some attributes of patent law, the Act was uniquely adapted to semiconductor mask works, in order to achieve appropriate protection for original designs while meeting the competitive needs of the industry and serving the public interest.

The Semiconductor Chip Protection Act arose from concerns that existing intellectual property laws did not provide adequate protection of proprietary rights in semiconductor chips that had been designed to perform a particular function. The Act, enacted after extensive congressional consideration and hearings over several years, adopted relevant aspects of existing intellectual property law, but for the most part created a new law, specifically adapted to the protection of design layouts of semiconductor chips.

Chip design layouts embody the selection and configuration of electrical components and connections in order to achieve the desired electronic functions. The electrical elements are configured in three dimensions, and are built up in layers by means of a series of "masks" whereby, using photographic depositing and etching techniques, layers of metallic, insulating, and semiconductor material are deposited in the desired pattern on a wafer of silicon. This set of masks is called a "mask work", and is part of the semiconductor chip product.

The statute defines a mask work as: a series of related images however fixed or encoded

- having or representing the predetermined, three dimensional pattern of metallic, insulating, or semiconductor material present or removed from the layers of a semiconductor chip product; and

[4] 17 U.S.C. Section 101.

[5] http://law.justia.com/cases/federal/appellate-courts.

- in which series the relation of the images to one another is that each image has the pattern of the surface of one form of a semiconductor chip product.

The semiconductor chip product [6] in turn is defined as the final or intermediate form of any product—

A) having two or more layers of metallic, insulating, or semiconductor material, deposited or otherwise placed on, or etched away or otherwise removed from, a piece of semiconductor material in accordance with a predetermined pattern; and

B) Intended to perform electronic circuitry functions.

The Semiconductor Chip Protection Act provides for the grant of certain exclusive rights to owners of registered mask works, including the exclusive right "to reproduce the mask work by optical, electronic, or any other means", and the exclusive right "to import or distribute a semiconductor chip product in which the mask work is embodied".

Mask works that are not "original", or that consist of "designs that are staple, commonplace, or familiar in the semiconductor industry, or variations of such designs, combined in a way that, considered as a whole, is not original", are excluded from protection. Protection is also not extended to any "idea, procedure, process, system, method of operation, concept, principle, or discovery, regardless of the form in which it is described, explained, illustrated or embodied" in the mask work".

The design of a satisfactory chip layout may require extensive effort and be extremely time consuming, particularly as new and improved electronic capabilities are sought to be created. A new semiconductor chip may incur large research and development costs, yet after the layout is imprinted in the mask work and the chip is available in commerce, it can be copied at a fraction of the cost to the originator. Thus there was concern that widespread copying of new chip layouts would have adverse effects on innovative advances in semiconductor technology.

Brooktree Corporation brought suit against Advanced Micro Devices, Inc. (herein AMD) for patent infringement[7], and infringement of mask work registrations[8], in connection with certain semiconductor chips used in colour video displays. The United States District Court for the Southern District of California entered judgment that the patents were valid and infringed and that the registered mask works were infringed, assessing damages.

Brooktree was granted mask work registration MW 2873 on August 6, 1987, and registration MW 3838 on July 6, 1988, for its chips identified as Bt451 and Bt458. These Brooktree chips embody a circuit design that combines the functions of a static random access memory (SRAM) and a digital to analog converter (DAC). This circuitry sometimes referred to as RAMDAC, acts as a "colour palette", producing the colours in colour video displays having high speed and enhanced picture resolution. A Brooktree witness described these chips as a technological breakthrough, exceeding limits in speed and performance that had been believed impossible to exceed. Brooktree stated that a single Bt458 chip replaced a previously used set of 36 chips (an AMD product) and offered many advantages. A Brooktree witness testified that these chips were extremely successful commercially, and were soon incorporated into new designs for video display systems made by several large manufacturers.

6 17 U.S.C. Section 901(a) (2).

7 35 U.S.C. Section 271.

8 17 U.S.C. Section 910.

A critical component of the Brooktree chips is the core cell, a ten-transistor SRAM cell which is repeated over six thousand times in an array covering about eighty percent of the chip area. Each core cell consists of ten transistors and metal conductors electrically connecting the transistors throughout the three dimensions of the multilayered cell. Brooktree charged that this core cell was copied by AMD, thus infringing Brooktree's mask work registrations.

AMD does not challenge the validity of these mask work registrations, or dispute Brooktree's position that its chips are protected under the Semiconductor Chip Protection Act. AMD does, however, assert that its accused chips are not infringements.....

The Semiconductor Chip Protection Act defines an "infringing semiconductor chip product" as one which is "made, imported, or distributed in violation of the exclusive rights" of the mask work owner[9]. The text of the Semiconductor Chip Protection Act sets forth the subject matter of protection in terms of certain exclusive rights, including, inter alia, the exclusive right to "reproduce the mask work"[10]. This usage mirrors the words of the Copyright Act, which states the exclusive rights of copyright owners "to reproduce the copyrighted work"[11]. Although the Semiconductor Chip Protection Act does not use the word "copy" to describe infringement, the parallel language reflects the incorporation of the well-explicated copyright principle of substantial similarity into the Semiconductor Chip Protection Act.

The jury instruction on the criteria for establishing infringement included the instruction that infringement requires substantial similarity to a material portion of the registered mask work:

To establish infringement, Brooktree must show that A.M.D.'s mask works are substantially similar to a material portion of the mask works in Brooktree's chips covered by Brooktree's mask work registration. No hard and fast rule or percentage governs what constitutes a, quote, "substantial similarity." Substantial similarity may exist where an important part of the mask work is copied, even though the percentage of the entire chip which is copied may be relatively small. It is not required that A.M.D. make a copy of the entire mask work embodied in the Brooktree chip.

AMD states that it does not on appeal challenge this jury instruction. Instead, AMD argues that because the non-SRAM portion of its accused chip was not copied, the chips are not "substantially similar", whatever the materiality of the SRAM cell to the total mask work. It was undisputed that there was not duplication of the entire chip. AMD states that the Semiconductor Chip Protection Act requires copying of the entire chip, and therefore that it was entitled to judgment in its favor as a matter of law, or at least to a new trial on the issue.

The principle of substantial similarity recognises that the existence of differences between an accused and copyrighted work may not negate infringement if a material portion of the copyrighted work is appropriated[12]. If the copied portion is qualitatively important, the finder of fact may properly find substantial similarity under copyright law (Baxter v. MCA, Inc[13]).

---

9 17 U.S.C. Section 901(a)(9).

10 17 U.S.C. Section 905.

11 17 U.S.C. Section 106.

12 *Shaw v. Lindheim, 919 F.2d 1353, 1362, 15 USPQ2d 1516, 1523 (9th Cir.1990).*

13 812 F.2d 421, 425, 2 USPQ2d 1059, 1063 (9th Cir.),

Brooktree agrees that the SRAM portion of the accused chips covers only eighty percent of the chip area, and that the remaining circuitry was not copied by AMD. Infringement under the statute does not require that all parts of the accused chip be copied. The district court's explanation to the jury was in full accord with the statutory grant of exclusive rights to reproduce the mask work. The statutory interpretation now pressed by AMD, viz., that the entire chip must have been copied, is unsupported. Indeed, the House Report states that it was contemplated that the cell layout alone could be misappropriated:

Mask works sometimes contain substantial areas of (so-called "cells") whose layouts involve creativity and are commercially valuable. In appropriate fact settings, the misappropriation of such a cell-assuming it meets the original standards of this chapter-could be the basis for an infringement action under this chapter

Although as a practical matter, copying of an insubstantial portion of a chip and independent design of the remainder is not likely, copying of a material portion nevertheless constitutes infringement. This concept is particularly important in the semiconductor industry, where it may be economical, for example, to copy 75% of a mask work from one chip and combine that with 25% of another mask work, if the copies are transferable modules, such as units from a cell library.

No hard and fast percentages govern what constitutes a "substantial" copying because substantial similarity may exist where an important part of a mask work is copied even though the percentage copied may be relatively small. Nonetheless, mask work owners are protected not only from wholesale copying but also against piecemeal copying of substantial or material portions of one or more mask works.

AMD's position at trial, and on appeal, was that its core cell was the product of reverse engineering of the Brooktree chip, and therefore does not constitute infringement under the Semiconductor Chip Protection Act. *Reverse engineering is a statutory defense, included in the Act upon extensive congressional attention to the workings of the semiconductor chip industry.*

Powtech v. Peak Technology Co. Ltd - *The first ruling to apply in the protection of Integrated Circuit Layout Design regulations in China.*

Ruling has been given on the lawsuit of Powtech against Peak Technology Co., Ltd ("Peak Technology") for the infringement of the integrated circuit layout design proprietary right by the Nanjing Intermediate People's Court of Jiangsu Province. The court applied the "Protection of Integrated Circuit Layout Design Regulations" and found that Peak Technology had violated the layout design proprietary right of Powtech and ruled in favor of Powtech request for stopping the infringement and claim for compensation for damages. It is said that it is the first case in China to apply the "Protection of Integrated Circuit Layout Design Regulations", setting a good example for protecting IC layout design of Chinese enterprises.

Powtech has been insisting on continuous innovation and focuses on LED lighting, LED backlight drivers and DC-DC converters IC design for years. The infringed product in the lawsuit, PT4115, is used as constant current high-power LED-drivers for LED lighting, which was granted an "integrated circuits layout design registration certification"

by the State Intellectual Property Office in July 2008. In April 2009, Powtech found that the defendant through reverse analysis acquired technical data of PT4115, including the specific electronic parameters, component structure, dimensions and interior design, and made imitations of it. The infringing products were sold in the market at low price. To protect its core interest against infringement, Powtech filed for court protection.

The IC design industry is a knowledge and technology driven industry. Intellectual property is the driver of sustainable development. Since its establishment, Powtech continuously invests resources in technology innovation to enhance in-depth research and development of LED technology. As at the end of August 2010, Powtech has 6 approved patents, 22 layout design protection registrations, and more than 10 patent applications. The purpose of the litigation is not only to deal a blow to illegal infringement, but also to demonstrate the determination in defending its intellectual property rights. Intellectual property protection of hi-tech companies relies on the macro-environment, which includes the industry's high awareness of proprietary right protection and sound legal system.

7.10 SUMMARY

- Cutting edge Innovations in semiconductor technologies have prompted the need to grant additional intellectual property protection for this particular form of investment in monetary and intellectual capital. The result has been the enactment of the Semiconductor Chip Protection Act in various countries.
- The legislative effort to fashion protection for chips focused on the "mask works." These are the series of masks that bear the circuit designs used to expose the photoresist in the fabrication process. Each mask bears the information that dictates which areas are to be exposed and which are to be covered during a given step in the process. Together, the masks describe the entire three-dimensional topography of the finished product.
- However, this focus was not inevitable. If the form of protection chosen for semiconductor chip products had been derived from patent law, more emphasis might have been placed, for example, on the fabrication process or on the product than on the intermediate masks.
- Initial proposals for a chip protection law called for an extension of copyright law, declaring mask works to be pictorial, graphic, and sculptural (PGS) works, notwithstanding their utilitarian purpose. Ordinarily, the design of a "useful article" is protectable as a PGS work only to the extent that it incorporates aspects that are physically or conceptually separable from their utilitarian aspects. The proposals would have created an exception to this limitation for mask works.
- However, as indicated, some felt that the forms of protection provided by existing versions of laws such as these did not suffice. For example, because of their utilitarian purpose, the layout designs of semiconductor chip products, whether embodied in masks or in the finished product, were not protected as pictorial, graphic, or sculptural works under copyright law. Also, although

some chip designs might be sufficiently novel and nonobvious to qualify for patent protection, it was felt that a great many would not. Finally, since the layout design of a chip can be observed by inspecting the final product, it would be difficult to maintain the requisite level of secrecy to qualify for trade secret protection once a chip is sold to the public. Consequently, the patent or copyright laws have been amended to enact a sui generis law.

- The *sui generis* law bears the basic features: narrow subject matter, 10-year term of protection, and a broad exception for reverse engineering. The foundation of the law was codified in one of its basic premises: that the technology was the fabrication of semiconductor chip products.
- The reverse engineering provisions are commonly mentioned in the industry as a primary reason that chip developers have brought few lawsuits under the act against copiers of their chip designs. This has been demonstrated in the cases of Brooktree Corporation v. Advanced Micro Devices. Protection for mask works is subject to several significant limitations, the most important of which is the reverse engineering exception.
- Another major weakness of the protection of ICs is the absence of any workable effective international protection. A sui generis law requires a *sui generis treaty* — a treaty that must be negotiated without any international consensus on what sort of regime for protection is appropriate. The primary multilateral effort to date was the Washington Treaty, prepared under the auspices of the World Intellectual Property Organisation (WIPO).
- However, the goal of the intellectual property laws is to give the public the benefit of innovative competition. It is also to curtail the practice that allows free riders to profit easily and cheaply from the success of others who make the R&D design investment and take the risks in bringing a new and innovative product to market.

7.11 TERMINAL QUESTIONS

1) What are the rights conferred by registration of IC under Semiconductor Integrated Circuit as per the SICLD Act 2000?
2) What happens when a chip lay out design is copied? How is the right holder protected under the SICLD Act 2000?
3) Write short notes on Infringement of Layout Design.

7.12 ANSWERS AND HINTS

Self Assessment Questions

1) Read Section 7.3
2) Read Section 7.1
3) Read Section 7.6

Terminal Questions

1) Read Section 7.4
2) Read Section 7.5 and 7.9
3) Read Section 7.5 and 7.9

7.13 REFERENCES AND SUGGESTED READINGS

Richard H. Stern, Semiconductor Chip Protection, *Harcourt Brace/Aspen Law & Business* (June 1985), ISBN 978-0317294132.

Symposium: *The Semiconductor Chip Protection Act of 1984 and Its Lessons, 70 Minn. L. Rev. 263 (1985)* - six law review articles on SCPA.

Baker, R. J. (2010): *CMOS-Circuit Design, Layout, and Simulation -Third Edition. Wiley-IEEE.* ISBN 978-0-470-88132-3 .

Hodges, D.A., Jackson H.G., and Saleh, R. (2003): *Analysis and Design of Digital Integrated Circuits.-McGraw-Hill.* ISBN 0-07-228365-7.

Rabaey, J.M., Chandrakasan, A., and Nikolic, B. (2003): *Digital Integrated Circuits-2nd Edition.* ISBN 0-13-090996-3

Mead, C. and Conway, L. (1980): *Introduction to VLSI Systems. Addison-Wesley.* ISBN 0-201-04358-0.

MIP-103-2-52-1000

MPDD-IGNOU/P.O. 1T March, 2017 (Reprint)

ISBN: 978-81-266-6265-4