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Course Design Committee

Prof. A. K. Ghatak, *Retd.*
IIT Delhi, New Delhi

Prof. Suresh Garg, *Retd.*
School of Sciences
IGNOU, New Delhi
Vice Chancellor,
Usha Martin University

Prof. R.M. Mehra, *Retd.*
Dept. of Electronics,
South Campus,
University of Delhi, Delhi

Dr. Ashok Goyal, *Retd.*
Dept. of Physics, Hansraj College
University of Delhi, Delhi

Dr. Parthasarathy
Dept. of Physics,
Maharaja Agrasen College,
University of Delhi, Delhi

Prof. M.S. Nathawat
Former Director,
School of Sciences,
IGNOU, New Delhi

Prof. Vijayshri
School of Sciences
IGNOU, New Delhi

Prof. Sudip Ranjan Jha
School of Sciences
IGNOU, New Delhi

Prof. Shubha. Gokhale
School of Sciences
IGNOU, New Delhi

Prof. Sanjay Gupta
School of Sciences
IGNOU, New Delhi

Dr. Subhalakshmi Lamba
School of Sciences
IGNOU, New Delhi

Course Preparation Team

Dr. Vijay Raybagkar, *Retd.*
(Experiments 4, 5, 10)
Dept. of Physics,
N. Wadia College, Pune

Prof. Shubha Gokhale
(Experiments 1 to 3, 6 to 9)
School of Sciences
IGNOU, New Delhi

Some of the Experiments in this course are based on the courses BPHL-103, PHE-08(L) and PHE-12(L) of the earlier B.Sc. programme of IGNOU.

Course Coordinators: Prof. Shubha Gokhale and Prof. Vijayshri

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AR (P), IGNOU

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DIGITAL AND ANALOG CIRCUITS AND INSTRUMENTATION: LABORATORY – INTRODUCTION

You got introduced to various aspects of Electronics in the theory course on Digital and Analog Circuits and Instrumentation (BPHCT-143). In this laboratory course you will be able to apply the principles, techniques and methods learnt in the theory course to perform various experiments. This laboratory course is closely related to the contents of the theory course, and hence we advise you to read the relevant units associated with respective experiments. (In the write-up of every experiment, we have mentioned the corresponding Unit in the theory course). Before going to perform any experiment in the laboratory at your Study Centre, we recommend that you should go through the relevant Units, in order to understand the experiment better and perform it with better efficiency.

This laboratory course contains 10 experiments.

In **Experiment 1** you will build the basic logic gates using the NAND gate, which is called a universal gate. In this experiment you will be introduced to the digital integrated circuit (IC) 7400, which contains four NAND gates within it. By making the proper connections to the different pins of the IC on a breadboard, you will build and test NOT, AND and OR gates.

In **Experiment 2** in the first part you will verify the de Morgan's theorems. In the second part you will minimise some given logic expressions using the Boolean relations and theorems. Then you will use different logic gate ICs to build the circuits to verify the truth tables of the original expressions and their minimised forms.

In **Experiment 3** you will build and test the half adder and full adder circuits using logic gate ICs.

To generate a rectangular wave of desired frequency with specific duty cycle (ON time of the pulse / TOTAL time), we use astable multivibrator circuit. In **Experiment 4**, you will build an astable multivibrator using IC 555, which is a well-known timer IC.

In **Experiment 5**, you will build a monostable multivibrator circuit using IC555. This circuit gives a single pulse of set duration, for every trigger signal given to the circuit.

Semiconductor junction diodes can be tailor-made by controlling their doping concentrations in the n - and p -regions. This gives rise to their peculiar I - V characteristics. Such special purpose diodes can be useful in various applications,. In **Experiment 6** you will work with two types of special purpose diodes, viz. a zener diode and a light emitting diode (LED). You will make proper biasing of these devices and record the forward and reverse bias characteristics of a zener diode and **only** forward bias characteristics of an LED.

Amplifiers are most commonly used circuits. Usually a bipolar junction transistor (BJT) is used as the amplifying element in an amplifier circuit. In **Experiment 7** you will study the input and output characteristics of a transistor. You will also design and build a class A amplifier using this transistor and measure its gain under different input signal frequencies.

Operational amplifier (op amp) is a versatile amplifier available in IC form. In **Experiment 8** you will use op amp IC 741 to build inverting and non-inverting amplifiers of specified gains. In **Experiment 9** you will build differentiator and integrator circuits using an op amp and observe the output waveforms of these circuits for different input waveforms like sine wave, square wave etc.

Generation of a sinusoidal wave from dc power supply is done with the help of an oscillator circuit. In **Experiment 10** you will design and build a phase shift oscillator of desired frequency and observe its output waveform.

We are sure that you will enjoy performing all these experiments in this laboratory course. You will learn different skills of electronic circuit design, assembly and testing.

We wish you all the best for performing the experiments of this laboratory course!



EXPERIMENT 1

REALISATION OF LOGIC GATES USING NAND GATES

Structure

1.1	Introduction Expected Skills	1.3	Obtaining Basic Logic Gates using NAND Gate Realisation of a NOT Gate Realisation of an AND Gate Realization of an OR Gate
1.2	Basics of Logic Gates		Appendix 1A: Details of Breadboard

1.1 INTRODUCTION

In the second block of theory course on Digital and Analog Circuits and Instrumentation (BPHET-143) you have learnt about digital electronics. You know that digital circuits are built using logic gates. In Unit 7 of that course you learnt that there are three basic types of gates namely AND, OR and NOT. You also learnt about the NAND, NOR, XOR and XNOR gates in that Unit. Out of these, NAND and NOR are called universal gates because by using these gates we can obtain all other types of gates.

In this experiment you will be building the three basic gates that is AND, OR and NOT gates using NAND gates. While performing this experiment you will get an opportunity to work with the digital ICs and use the breadboard to build the circuits. You will get familiarised with the necessary power supplies required to build digital circuits as well as learn the precautions to be taken while handling the integrated circuits.

Expected Skills

After doing this experiment, you should be able to:

- ❖ identify the digital ICs by their number;
- ❖ use the breadboard to build a circuit using digital ICs;
- ❖ handle the digital ICs taking due precautions;
- ❖ choose proper power supply for digital circuits;
- ❖ build a NOT gate using NAND gate and verify its truth table;
- ❖ build an AND gate using NAND gates and verify its truth table; and
- ❖ build an OR gate using NAND gates and verify its truth table.

For doing this experiment, you will require the following apparatus and components.

Apparatus Required

Digital IC 7400; $\pm 5V$ power supply; a breadboard; connecting wires and a voltmeter or a multimeter in dc voltage measurement mode.

1.2 BASICS OF LOGIC GATES

In Unit 7 of the theory course on Digital and Analogue Circuits and Instrumentation (BPHE-143) you have learnt about the basic logic gates, their symbols and truth tables. However for completeness, here we recapitulate in brief the circuit symbols and truth tables of AND, OR, NOT and NAND gates.

In Fig. 1.1 the circuit symbol of OR gate is shown along with its truth table.

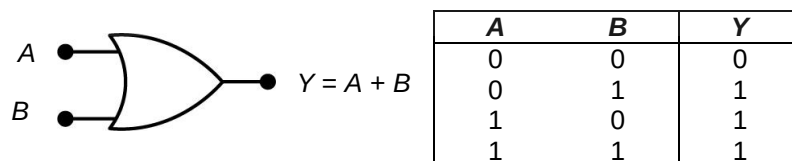


Fig. 1.1: Circuit symbol and truth table of OR gate.

From the truth table you can see that whenever either or both the inputs of OR gate are 1 (or high), then its output is high.

In Fig. 1.2 the circuit symbol and truth table of an AND gate is shown.

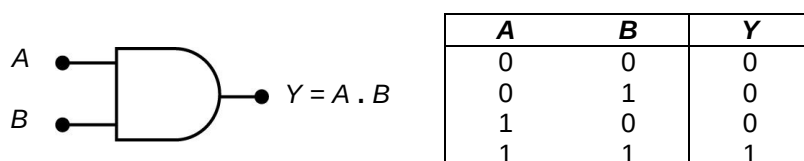


Fig. 1.2: Circuit symbol and truth table of AND gate.

Here only when both the inputs of AND gate are high, then the output is 1 or high, otherwise the outputs are 0 (or low).

The circuit symbol and the truth table of NOT gate is shown in Fig. 1.3.

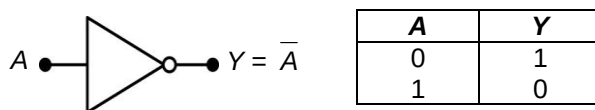


Fig. 1.3: Circuit symbol and truth table of NOT gate.

As you know, the NOT gate has only single input and a single output, and the signal given at the input is inverted at the output.

In this experiment you are going to use only one type of gate for building all the about three logic gates. It is the NAND gate. You know that it is a combination of an AND gate followed by a NOT gate. Its circuit symbol and truth table is shown in Fig. 1.4.

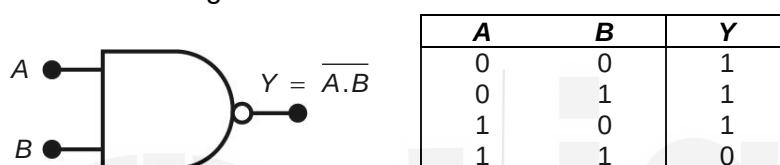


Fig. 1.4: Circuit symbol and truth table of NAND gate.

In NAND gate whenever any of the inputs is 0 or low, the output is high. Only when both the inputs are 1, the output is 0.

You have already learnt that the logic gates are built in the form of integrated circuits i.e. IC. Each of the IC is a collection of logic gates within it and is identified by a particular number. In this experiment you are going to use the NAND gate IC to build the other gates. The most commonly used NAND gate is IC 7400 which contains four NAND gates with 2-inputs and one-output each, hence it is called a *quad* 2-input NAND gate IC. There are other variants of NAND gate ICs like dual NAND gate IC containing 2 NAND gates or a triple NAND gate IC containing 3 NAND gates. But 7400 is the most popular IC. There are various manufacturers of the integrated circuits, however all of them use the same number codes as well as pin-out connection. IC 7400 is usually available in dual in-line pack with 14 pins. The pin-out diagram of IC 7400 is given in Fig. 1.5. Here the inputs of four NAND gates are designated at 1A-1B, 2A-2B, 3A-3B and 4A-4B. The respective outputs are indicated as 1Y, 2Y, 3Y and 4Y.

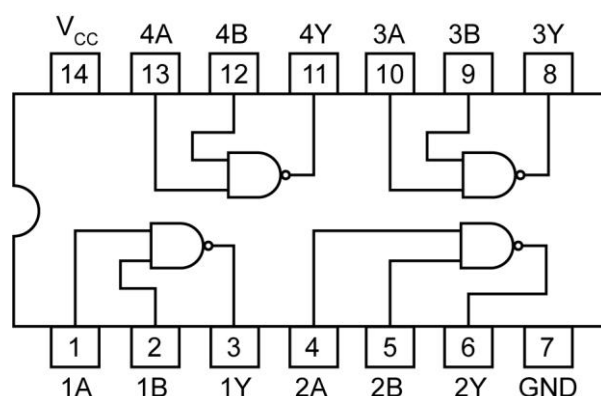


Fig. 1.5: Pin-out diagram of 7400 quad 2-input NAND gate IC.

There are two more pins used for supplying the voltage to the IC. Pin number 14 is connected to + 5V supply whereas pin number 7 is connected to the ground.

With this background now you can start performing the experiment in which you will build different basic gates using this IC.

1.3 OBTAINING BASIC LOGIC GATES USING NAND GATE

For performing the experiment, you will assemble the circuit on a breadboard which has an arrangement of connecting lines as described in Appendix-1A. On the breadboard you will insert the IC in the middle rails and make the connections using single strand connecting wires. You will require a power supply giving + 5V. On the breadboard you will choose one of the horizontal rails to connect to positive terminal of the supply and another one for the ground terminal of the supply.

Now we will describe the procedure to build the basic logic gates one by one.

1.3.1 Realisation of a NOT Gate

The NOT gate can be obtained using just one NAND gate, as shown in Fig. 1.6. Here both the inputs of the NAND gate are connected together and the input signal is given to these shorted inputs of the NAND gate.



Fig. 1.6: Realisation of NOT gate using NAND gate.

Here the input A is fed to both the inputs of the NAND gate and the output Y is a complement or inverted output of an AND gate i.e. $\overline{A \cdot A} = \overline{A}$.

Procedure

To build and verify this circuit proceed with the following steps:

1. Connect the two inputs of a NAND gate [say pin numbers 1(1A) and 2(1B)] together as shown in the circuit.
2. Connect the power supply as described earlier i.e. the positive terminal of the power supply (+ 5V) to pin number 14 and the ground terminal to pin number 7. The circuit will look similar to the one shown in Fig. 1.7.
3. Connect the voltmeter or a multimeter (in dc volts mode) to the output of the NAND gate that is pin number 3 (1Y) in our example. In some cases,

you may also be able to use LED as indicators of 'HIGH' and 'LOW' state of the output in place of a voltmeter. In such case make the circuit connections under the guidance of your counsellor.

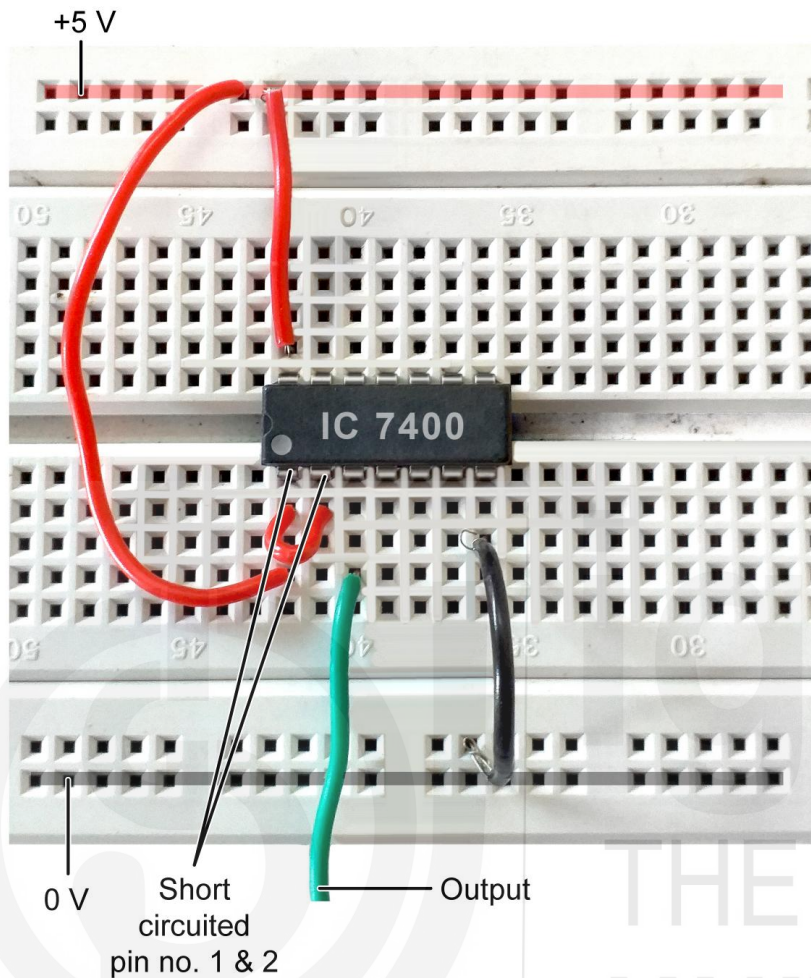


Fig. 1.7: Assembled circuit of NOT gate using IC 7400 on the breadboard.

4. Connect the + 5V line i.e. high signal to pin number 1 (input 1A shorted with 1B).
5. Switch *ON* the power supply.
6. Read the voltage in the voltmeter (output 1Y).
7. Enter the readings of input and output voltages in Observation Table 1.1.
8. Switch *OFF* the power supply.
9. Now remove the input wire from + 5V and connect it to the ground.
10. Switch *ON* the power supply.
11. Measure the output voltage.
12. Enter the input and output voltages in Observation Table 1.1.
13. Switch *OFF* the power supply.

You will note voltage > 4V as '1' and less than 0.8 V as '0' in the Observation Table.

Observation Table 1.1: Truth table of NOT gate built using a NAND gate

A	Y
1	...
0	...

From the Observation Table 1.1 verify that the circuit you have built is acting like a NOT gate.

1.3.2 Realisation of an AND Gate

It is quite simple to get an AND gate from NAND gates because from the truth tables of these two gates you will realise that the output of a NAND gate is essentially an inverse of the output of an AND gate. Hence by cascading 2 NAND gates as shown in Fig. 1.8, you can obtain an AND gate. Here the inputs are given to the first NAND gate and its output is given to the input of another NAND gate whose inputs are shorted together. The second gate is acting as a NOT gate here.

You will follow the similar procedure that you used in verifying the NOT gate.

**Fig. 1.8: Implementation of AND gate using NAND gates.**

Procedure

To perform this part of the experiment, you can start off with the circuit that you built for NOT gate.

1. As is evident from the circuit diagram shown in Fig. 1.8, we need 2 NAND gates to build an AND gate. In the last part of the experiment you have already built a NOT gate.
2. Now you have to apply the two inputs to another NAND gate. For example, you choose input pins 9 (3B) and 10 (3A) for applying the input signals of your AND gate. Then output of that NAND gate i.e., pin number 8 (3Y) should be connected to the input of the NOT gate, i.e. pin number 1 or 2 which are shorted together.
3. The voltmeter to verify the output of your circuit continues to remain at the output of the NOT gate, i.e., at pin number 3 (1Y).
4. Once all the connections are done and checked by your counsellor, you can start obtaining the truth table of the circuit you have prepared.
5. You have to apply the inputs at pin number 9 and 10, as per the Observation Table 1.2. For various combinations of inputs you should

measure the voltage at the output i.e. at pin number 3, which is the output of the NOT gate.

Observation Table 1.2: Truth table of an AND gate built using NAND gates

A (Pin 10)	B (Pin 9)	Y (Pin 3)
0	0	
0	1	
1	0	
1	1	

- Verify that the input and output noted in Observation Table 1.2 are matching with the truth table of the AND gate.
- Turn OFF the power supply.

Now you will learn to build an OR gate using NAND gates.

1.3.3 Realisation of an OR Gate

To build an OR gate using NAND gates refer to Fig. 1.9. You will notice that here we are using the de Morgan's theorem to get the OR gate.

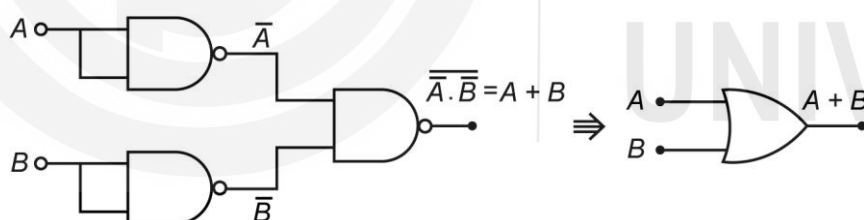


Fig. 1.9: OR gate using NAND gates.

You will require in all 3 NAND gates. First two NAND gates are used to invert the input signals, i.e., they are used in NOT gate configuration. And the output of the two NOT gates are given to the third NAND gate. By applying the de Morgan's theorem ($\overline{AB} = \overline{A} + \overline{B}$) and the Boolean identity $\overline{\overline{X}} = X$, the output of the third NAND gate will give you the output in the form of an OR gate.

Procedure

- Connect two NAND gates in the configuration of NOT gates as done in the first part of the experiment. For example, you can short pin number 1 and 2 and take output at pin number 3 as one of the inputs for the last NAND gate, say, pin number 10. Similarly, the second input for the last NAND

gate can be obtained by shorting the inputs of second NAND gate, i.e. pin numbers 4 and 5 and taking its output (at pin number 6) as the second input of the last NAND gate at pin number 9.

2. Connect all the three gates as described above and get the circuit checked by your counsellor.
3. Apply the inputs to the two NOT gates as various combinations of 0's and 1's as listed in Observation Table 1.3. Verify the output by connecting a voltmeter to the output of the last NAND gate, at pin number 8.

Observation Table 1.3: Realisation of OR Gate using NAND gates

A	B	$Y = \overline{\overline{A} \cdot \overline{B}} = A + B$
0	0	
0	1	
1	0	
1	1	

In this way you have built basic logic gates using NAND gate and verified their truth tables.

In the next experiment you will build more complicated logic circuits using some other digital ICs.

APPENDIX 1A: DETAILS OF BREADBOARD

A Breadboard is widely used in electronics laboratories to try out some temporary circuits. There is no need of soldering so it is easy to change components and connections. The components are not damaged and can be re-used.

Fig. 1A.1 shows a photograph of a typical breadboard which is commonly used for building simple circuits.

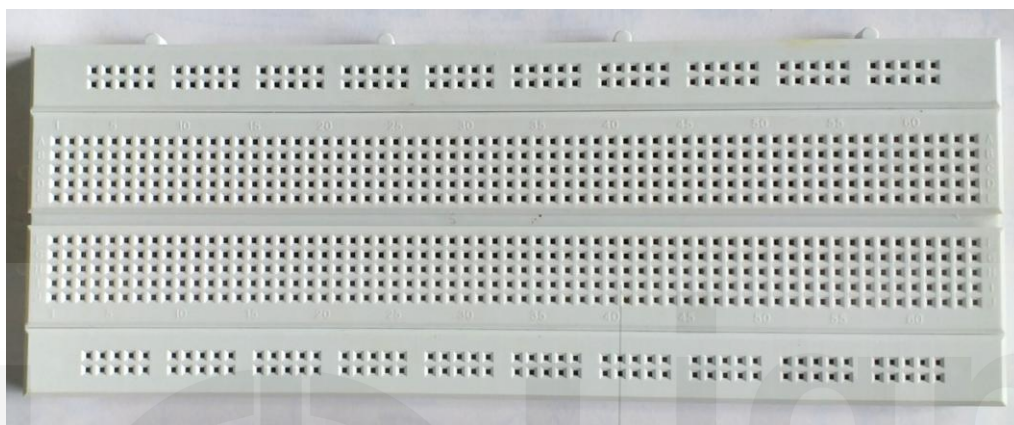


Fig. 1A.1: A typical breadboard.

Connections on the Breadboard

Breadboards have many small holes arranged on a 0.1" grid. The leads (connecting wires) of the components can be easily pushed into the holes. ICs are inserted across the central gap with their notch or dot to the left.

Fig. 1A.2 shows how the holes on the breadboard are internally connected.

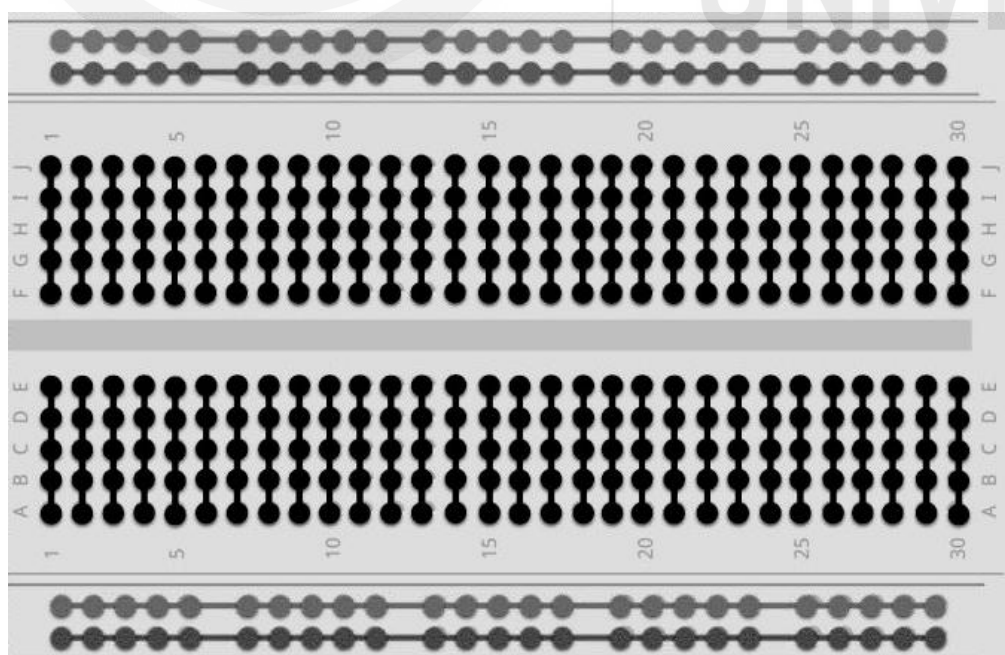


Fig. 1A.2: Internal connections on a breadboard.

The top and bottom two rows are connected **horizontally** all the way across as shown by the horizontal lines in the figure. The power supply is connected to these rows.

The other holes are linked **vertically** in blocks of 5. There is no link across the centre as shown by the gray line in the middle of the figure. So, if the IC is placed in the holes around this middle portion, there are separate blocks of connections to each pin of the IC.



EXPERIMENT 2

MINIMISATION OF LOGIC CIRCUITS

Structure

- | | | | |
|-----|---|-----|--|
| 2.1 | Introduction
Expected Skills | 2.3 | Verification of the de Morgan's Theorems |
| 2.2 | Familiarisation with Basic Logic Gate ICs | 2.4 | Simplification of Logic Expressions
Simplifying $Y = (A + B) \overline{AB}$
Simplifying $Y = \overline{AB} + (\overline{A} + \overline{B}) \overline{C}$
Simplifying $Y = \overline{AC} + AB(\overline{B} + C)$ |

2.1 INTRODUCTION

In the last experiment you learnt to build basic logic gates using NAND gate. In this experiment you will get acquainted with the ICs available for different basic logic gates and use them for building a logic circuit based on the logic expressions. You will use these logic circuits to verify some of the important Boolean laws and theorems. You will also learn to minimise complicated logic equations and build the logic circuits to verify the truth tables of original logic expressions and their minimised versions.

In the last experiment you used a quad 2-input NAND gate IC 7400 extensively. In this experiment you will use some more ICs containing basic logic gates. These ICs are typically,

1. IC 7432 : Quad 2-input OR gate
2. IC 7408 : Quad 2-input AND gate
3. IC 7404 : Hex inverter

There are other number of ICs also performing similar functions, but we will describe only these ICs here. If some other equivalent ICs are given to you in the laboratory, then contact your counsellor to get their details like pin-out diagrams and supply voltage requirement.

You will use these ICs to build the circuits represented by logic expressions.

Expected Skills

After performing this experiment, you should be able to:

- ❖ use IC 7404, 7408 and 7432 to build logic circuits;
- ❖ verify de Morgan's theorems;
- ❖ minimise the given logic expression using Boolean laws and theorems; and
- ❖ verify the truth tables of logic expressions and their minimised versions.

To perform this experiment, you will require the following components.

Apparatus Required

ICs 7404, 7408, 7432; breadboard; connecting wires; power supply of +5V; voltmeter or multimeter.

2.2 FAMILIARISATION WITH LOGIC GATE ICs

In the last experiment you used the NAND gate IC which contained 4 NAND gates within it. Similarly there are ICs corresponding to AND gates, OR gates and NOT gates.

In Fig. 2.1 we have shown the pin-out diagram of IC 7432 which comprises four OR gates.

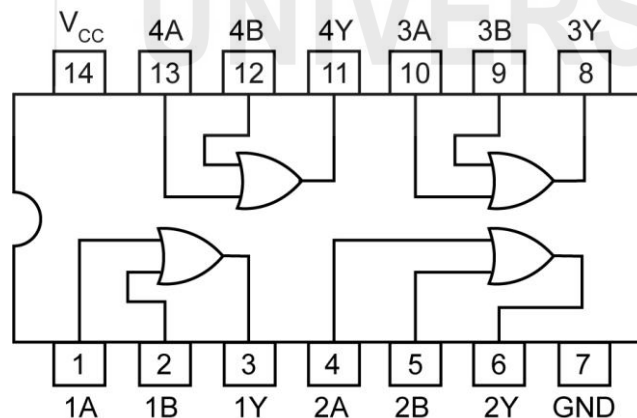


Fig 2.1: Pin-out diagram of quad 2-input OR gate IC 7432.

Similar to IC 7400 the supply is given to pin number 14 and pin number 7 is grounded. The input and outputs of the four OR gates are depicted in the figure by gate numbers 1, 2, 3 and 4, with respective inputs 1A-1B, 2A-2B, 3A-3B and 4A-4B. The respective outputs are indicated as 1Y, 2Y, 3Y and 4Y.

In Fig. 2.2 We have shown the pin-out diagram of IC 7408.

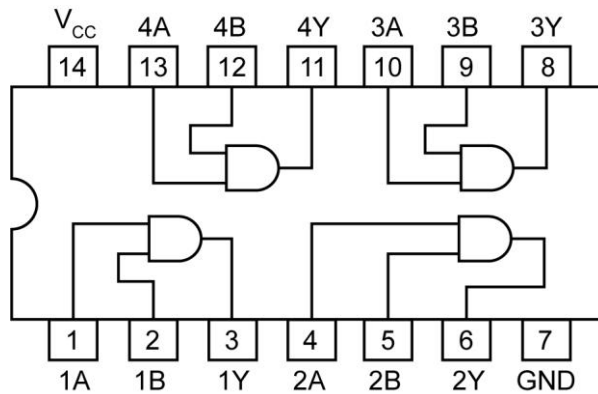


Fig 2.2: Pin-out diagram of quad 2-input AND gate IC 7408.

It contains four AND gates of 2-inputs each. The power supply is connected between pin number 14 and pin number 7 similar to the other ICs.

As you know, the NOT gate has only one input and one output terminal. Hence in a 14-pin dual in-line pack IC we get six NOT gates. In Fig. 2.3 we have shown the pin-out diagram of Hex inverter IC 7404.

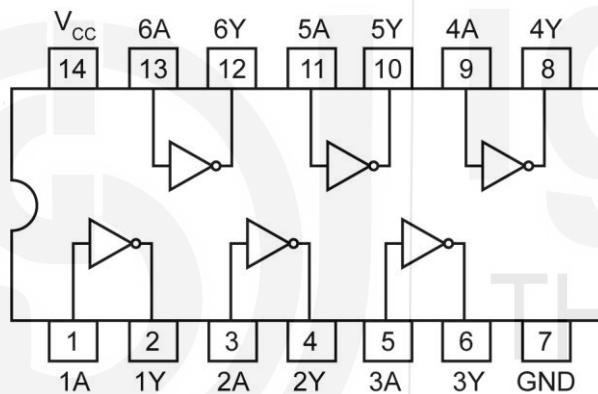


Fig 2.3: Hex inverter IC 7404.

Here also the power supply is provided between pin numbers 14 and 7 while the inputs and outputs of the six NOT gates are as indicated.

In this experiment you will make use of all these ICs.

Now that you are familiar with the basic logic gate ICs, you can start your experiment. In the first part you will verify the de Morgan's theorems and in the second part you will simplify some logic expressions. For this experiment you should study Units 7 and 8 of the theory course on Digital and Analogue Circuits and Instrumentation (BPHE-143) very carefully.

2.3 VERIFICATION OF THE de MORGAN'S THEOREMS

You have learnt in Unit 7 of the theory course BPHE-143 that there are two de Morgan's theorems:

$$\overline{X + Y} = \overline{X} \cdot \overline{Y} \quad (2.1)$$

$$\overline{X \cdot Y} = \overline{X} + \overline{Y} \quad (2.2)$$

These are very useful in simplifying the Boolean expressions. Now you will build a circuit using the ICs described above to verify both these theorems.

To verify the first theorem you have to build the circuit to get $\overline{X+Y}$ and generate its truth table. Then you will build a circuit to get $\overline{X} \cdot \overline{Y}$, obtain its truth table and compare it with the truth table of the circuit corresponding to the left hand side of Eq. (2.1).

Procedure

1. Take one quad 2-input OR gate IC 7432 and one hex inverter IC 7404. Connect them as shown in Fig. 2.4 on a breadboard.

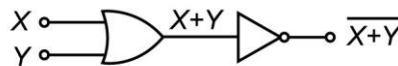


Fig. 2.4: Circuit to build $\overline{X+Y}$.

2. Give the power supply to both the ICs by connecting + 5V to pin number 14 and ground terminal to pin number 7.
3. The inputs are to be given to the two inputs of any one of the OR gates of IC 7432, (say) to pin number 1 and 2. The output of this OR gate, i.e., pin number 3 is to be connected to the input of the NOT gate i.e., say, number one of IC 7404.
4. Connect the voltmeter or multimeter (in dc voltage measurement mode) to pin number 2 of IC 7404, i.e., the output of the NOT gate.
5. Switch on the power supply. Now apply different combinations (0's and 1's) of inputs to the OR gate as per the Observation Table 2.1. Note down the output for each combination of inputs. Record your readings under the third column in Observation Table 2.1 that is for $\overline{X+Y}$.
6. Switch off the power supply.
7. Now, disconnect the OR and NOT ICs and choose one AND gate i.e. IC 7408 and a NOT gate IC 7404.
8. Connect the ICs 7408 and 7404 on the breadboard as shown in Fig. 2.5.

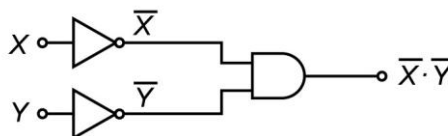


Fig. 2.5: Circuit to build $\overline{X} \cdot \overline{Y}$.

Here we are going to use two NOT gates and one AND gate. The two inputs X and Y are given to two NOT gates and the outputs of these two NOT gates are given to the two inputs of the AND gate.

9. Apply + 5V at pin number 14 and ground connection to pin number 7 of the ICs, and switch on the power supply.

10. Again apply the different combinations of inputs that is 0's and 1's to this circuit and note down the output in each case. Record your results in the last column of Observation Table 2.1.

Observation Table 2.1: Verification of de Morgan's first theorem

X	Y	$\overline{X+Y}$	$\overline{X} \cdot \overline{Y}$
0	0		
0	1		
1	0		
1	1		

11. Compare the outputs recorded in the 3rd and 4th column of Observation Table 2.1. They should be the same. This verifies de Morgan's first theorem.

If your results in both the columns are not matching then consult your counsellor.

Now you can proceed to verify the second theorem i.e. $\overline{X \cdot Y} = \overline{X} + \overline{Y}$.

Here you will be using an AND gate and a NOT gate to generate the truth table of the left hand side of the expression while you will require two NOT gates and an OR gate to verify the right hand side of the expression.

The circuits you require for verifying this theorem are shown in Fig. 2.6a and 2.6b.

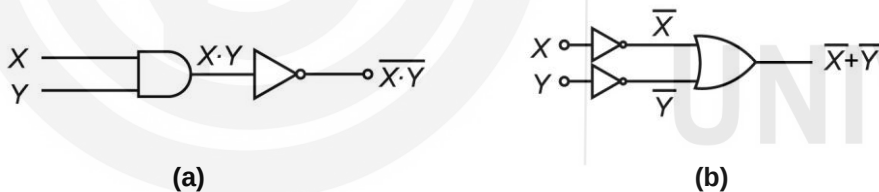


Fig. 2.6: a) Circuit to realise $\overline{X \cdot Y}$; b) Circuit to realise $\overline{X} + \overline{Y}$.

You should follow the similar procedure that you used for verifying the first theorem and generate the Observation Table 2.2. You should verify that the outputs of both the circuits are matching. This will verify de Morgan's second theorem.

Observation Table 2.2: Verification of de Morgan's second theorem

X	Y	$\overline{X \cdot Y}$	$\overline{X} + \overline{Y}$
0	0		
0	1		
1	0		
1	1		

After verifying the de Morgan's theorems now proceed to realise the logic circuits for the given Boolean expressions and their minimised versions.

2.4 SIMPLIFICATION OF LOGIC EXPRESSIONS

In Unit 8 of the theory course on Digital and Analog Circuits and Instrumentation (BPHEL-143) you had come across complicated logical expressions which were simplified using the Boolean laws and theorems. In this part of the experiment you will work with 3 Boolean expressions, minimise them using Boolean laws and theorems and experimentally verify that the minimisation also results into the same output as the original expression.

For this you will a) build a circuit for the logical expression by using logic gate ICs, b) verify their truth tables, c) workout the minimisation of the expression using Boolean laws and theorems, d) build the logic circuit corresponding to the minimised version, e) obtain its truth table, and f) compare the two truth tables.

You will be working with the following three expressions:

1. $Y = (A + B) \overline{AB}$
2. $Y = \overline{AB} + (\overline{A} + \overline{B}) \overline{C}$
3. $Y = \overline{AC} + AB(\overline{B} + C)$

For working with all these three expressions you will be using combinations of OR gate, AND gate and NOT gate ICs. You should build the circuit just the way you did for the other parts of the experiment and verify the output of the circuit for different combinations of a input and report them in the Observation Tables.

2.4.1 Simplifying $Y = (A + B) \overline{AB}$

To build a circuit for the expression $Y = (A + B) \overline{AB}$ you will use one OR gate, two AND gates and 1 NOT gate as shown in Fig. 2.7.

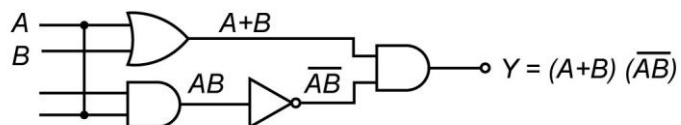


Fig. 2.7: Circuit for implementing $(A + B) \overline{AB}$.

You will build a circuit using ICs 7404, 7408 and 7432. Then apply different combinations of inputs A and B and record the outputs in Observation Table 2.3.

You can simplify this expression using the de Morgan's theorem in the following steps:

$$\begin{aligned}
 Y &= (A + B)(\overline{AB}) \\
 &= (A + B)(\overline{A} + \overline{B}) \\
 &= A\overline{A} + A\overline{B} + B\overline{A} + B\overline{B} = A\overline{B} + \overline{A}B
 \end{aligned}$$

You can implement the expression $(A\overline{B} + \overline{A}B)$ using two NOT gates two AND gates and one OR gate as shown in Fig. 2.8.

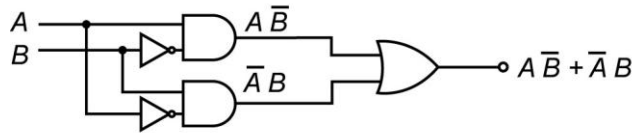


Fig. 2.8: Implementation of $A\overline{B} + \overline{A}B$.

Connect this circuit and verify its output for different combinations of inputs A and B. Record your results in the last column of Observation Table 2.3.

Observation Table 2.3: Output of $Y = (A + B)\overline{AB}$ and $Y = \overline{AB} + \overline{A}B$

A	B	$Y = (A + B)\overline{AB}$	$Y = \overline{AB} + \overline{A}B$
0	0		
0	1		
1	0		
1	1		

You should get the same outputs for both the circuits. You must have realised that this expression corresponds to an exclusive-OR (XOR) gate.

2.4.2 Simplifying $Y = \overline{AB} + (\overline{A} + \overline{B})\overline{C}$

The circuit depicting the expression $Y = \overline{AB} + (\overline{A} + \overline{B})\overline{C}$ shown in Fig. 2.9.

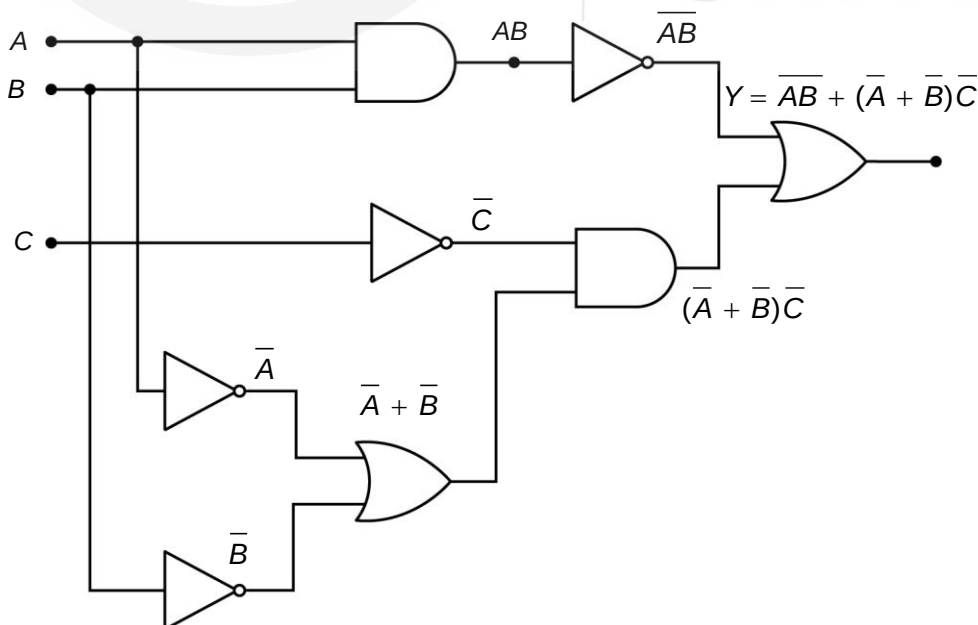


Fig. 2.9: Circuit for the expression $Y = \overline{AB} + (\overline{A} + \overline{B})\overline{C}$.

You should build the circuit using 2 AND gates, 4 NOT gates and 2 OR gates and record the truth table in Observation Table 2.4.

Using the Boolean laws and theorems given in Unit 7 of the theory course, you can minimise this expression in the following steps:

$$\begin{aligned}
 Y &= (\bar{A} + \bar{B})C + \bar{A}\bar{B} \\
 &= (\bar{A} + \bar{B})C + (\bar{A} + \bar{B}) \quad \text{Using de Morgan's 2nd theorem 26} \\
 &= (\bar{A} + \bar{B})(C + 1) \quad \text{Taking } (\bar{A} + \bar{B}) \text{ common} \\
 &= (\bar{A} + \bar{B}).1 = \bar{A} + \bar{B} \quad \text{Using Theorems 7 and 3}
 \end{aligned}$$

So the minimised expression is $Y = \bar{A} + \bar{B}$. The circuit realising this expression is shown in Fig. 2.10.

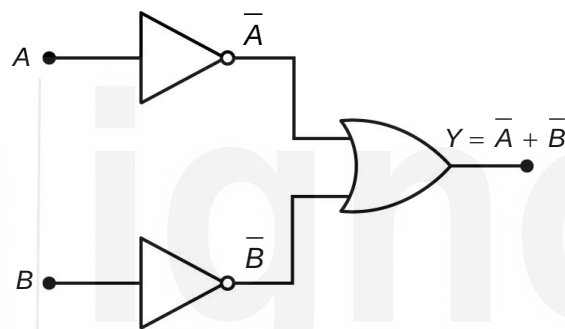


Fig. 2.10: Digital circuit for $Y = \bar{A} + \bar{B}$.

Here you require only two NOT gates followed by an OR gate to build the circuit. In this case there is no C input and any value of C is not going to change the output in the truth table. You should record your observations in Observation Table 2.4. For every value of input you should measure the output for circuit shown in Fig. 2.9 and also corresponding output for circuit shown in Fig. 2.10. You will realise that the output are matching. This verifies that the minimised form of the expression is correct.

Observation Table 2.4: Minimisation of expression $Y = \bar{A}\bar{B} + (\bar{A} + \bar{B})\bar{C}$

A	B	C	$Y = \bar{A}\bar{B} + (\bar{A} + \bar{B})\bar{C}$	$Y = \bar{A} + \bar{B}$
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Result: Are the outputs of the original expression and its minimised form the same?

2.4.3 Simplifying $Y = \bar{A}C + AB(\bar{B} + C)$

The circuit to realise $Y = \bar{A}C + AB(\bar{B} + C)$ is shown in Fig. 2.11.

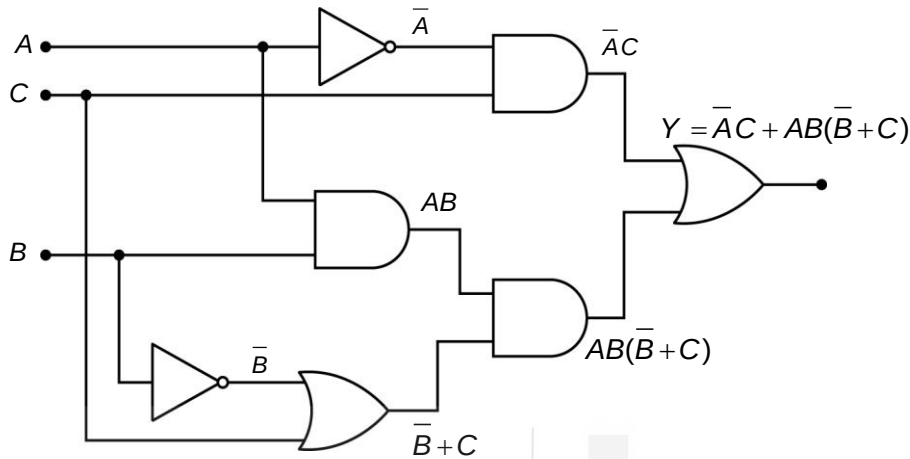


Fig. 2.11: Circuit to implement $Y = \bar{A}C + AB(\bar{B} + C)$.

To build this circuit you will require 2 NOT gates, 3 AND gates and 2 OR gates. So you will use ICs 7404, 7408 and 7432.

Build the circuit using these three ICs on the breadboard. Give various combinations of 0's and 1's at the inputs A, B, C and note the corresponding outputs in Observation Table 2.5.

You can minimize the expression using Boolean laws and theorems in following steps:

$$\begin{aligned}
 Y &= \bar{A}C + AB(\bar{B} + C) = \bar{A}C + AB\bar{B} + ABC \\
 &= \bar{A}C + A.0 + ABC && \text{Using Theorem 10} \\
 &= \bar{A}C + ABC && \text{Using Theorem 1} \\
 &= (\bar{A} + AB)C && \text{Taking C common} \\
 &= (\bar{A} + B)C && \text{Using Theorem 23} \\
 &= \bar{A}C + BC && \text{Using Theorem 7}
 \end{aligned}$$

Hence, $Y = \bar{A}C + BC$ is the minimised form of the logic expression. Now build a circuit to realise this expression as shown in Fig. 2.12.

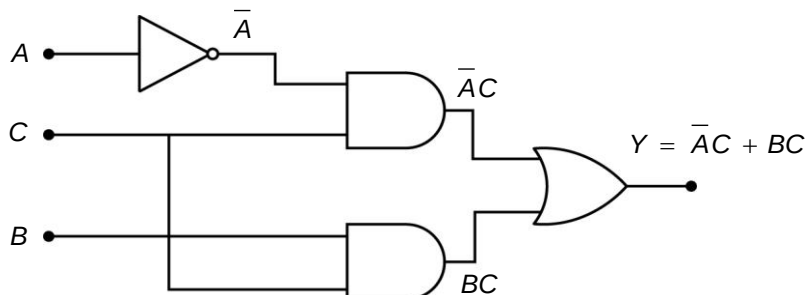


Fig. 2.12: Realisation of $Y = \bar{A}C + BC$.

To build this circuit you will require just 1 NOT gate, 2 AND gates and 1 OR gate. Assemble this circuit on the breadboard using ICs 7404, 7408 and 7432. Give various combinations of inputs (0's and 1's) and note down the corresponding outputs in the last column of Observation Table 2.5.

Observation Table 2.5: Minimisation of $Y = \bar{A}C + AB(\bar{B} + C)$

A	B	C	$Y = \bar{A}C + AB(\bar{B} + C)$	$Y = \bar{A}C + BC$
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Compare and verify that the outputs of both the circuits are matching.

EXPERIMENT 3

REALISATION OF ADDER CIRCUITS USING LOGIC GATES

Structure

- | | | | |
|-----|-----------------|-----|------------|
| 3.1 | Introduction | 3.3 | Full Adder |
| | Expected Skills | | |
| 3.2 | Half Adder | | |

3.1 INTRODUCTION

In the last two experiments you got introduced to the logic gates and you built different logic circuits using digital ICs. In this experiment you will work with some applications of logic gates. The main application of the logic gates is the Adder Circuits. In Unit 9 of the theory course on Digital and Analog Circuits and Instrumentation (BPHET-143) you have learnt the theory about the half adder and full adder circuits. In this experiment you will build these two adder circuits using digital ICs. You know that the half adder circuit is used for summing up 2 bits in binary form. It has two inputs and the two outputs called the Sum and the Carry. In the full adder circuit you can add 3 bits and obtain the output in the form of Sum and Carry. In the half adder circuit the sum is obtained using an XOR while the carry is obtained using an AND gate. The full order can be implemented using two half adders or a 3-input XOR gate.

Expected Skills

After performing this experiment, you should be able to:

- ❖ draw the circuit of half adder and write its truth table;
- ❖ build the circuit of half adder using NAND gates and obtain the sum and carry outputs;
- ❖ verify the truth table of half adder;
- ❖ draw the circuit of full adder using only NAND gates;
- ❖ build the circuit of the full adder using NAND gates; and
- ❖ verify the truth table of full adder.

To perform this experiment, you will require the following components.

Apparatus Required

ICs 7400 – 5 no.; breadboard; connecting wires; power supply of + 5V; two voltmeters or multimeters in dc voltage measurement mode.

3.2 HALF ADDER

In Unit 9 of theory course on Digital and Analog Circuits and Instrumentation, you have extensively studied about the half adder. Here we give the only essential points for ready reference. The truth table of the half adder is given in Table 3.1.

Table 3.1: Truth table of half adder

A	B	Carry	Sum
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

You can easily see that the sum is obtained by performing an XOR function, while the carry is obtained by an AND operation. The circuit diagram representing the half adder is shown in Fig 3.1.

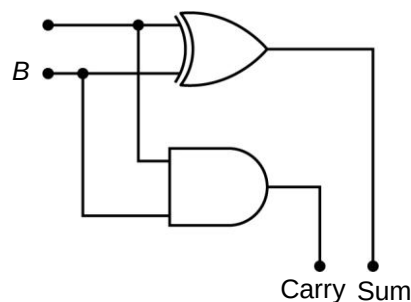


Fig. 3.1: Circuit for half adder.

Now you have to obtain the sum part and the Carry part using only NAND gates. You have already done this in the first experiment. However in Fig. 3.2a we show the circuit required to build an XOR gate using only the NAND gates, and in Fig. 3.2b the circuit to get an AND gate from NAND gate.

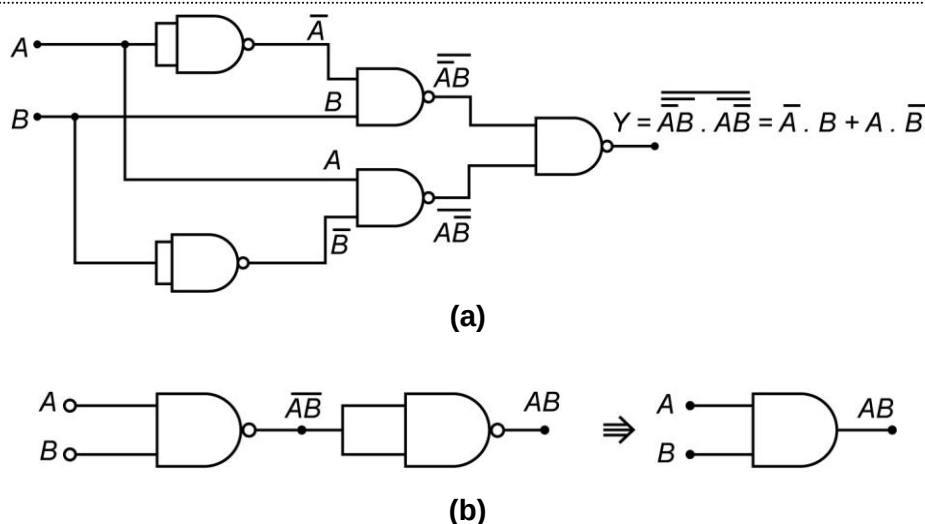


Fig. 3.2: a) XOR gate using NAND gates to get the Sum; b) AND gate using NAND gates to get the Carry.

It is clear from Fig. 3.2a that you need 5 NAND gates to build an XOR gate and two for an AND gate. In this way to build a half adder you will require 7 NAND gates. Now you are aware that IC 7400 is a quad NAND gate IC. It means that there are only 4 NAND gates in it. So you will need 2 NAND gate IC 7400 to perform this part of the experiment. After understanding the circuits to be built perform the following procedure to complete the experiment.

Procedure

1. Take a breadboard and place two IC 7400 on it.
2. Give + 5V supply to pin number 14 of both the ICs and connect Pin number 7 of both ICs to ground.
3. Refer to Fig. 3.2a and build an XOR gate using four NAND gates from the left hand side IC 7400 and one NAND gate from the second IC. This will form the sum output of the half adder.
4. Build a AND gate using any two of the remaining 3 NAND gates of the second IC 7400. This is the carry output of the half adder.
5. Now you have to give same inputs A and B to both the parts of the circuit that is to the Sum (XOR) circuit as well as the Carry (AND) circuit.
6. Apply different combinations of 0's and 1's to the inputs A and B as given in the Observation Table 3.2 and measure the voltages at both Sum and Carry outputs and record them in the Observation Table.

Observation Table 3.2: Truth table of half adder built using NAND gates

A	B	Carry	Sum
0	0		
0	1		
1	0		
1	1		

7. Verify the truth table recorded by you in the Observation Table 3.2 with the truth table given in Table 3.1.

3.3 FULL ADDER

You have learnt about the full adder in Unit 9 of the theory course on Digital and Analog Circuits and Instrumentation. With this adder we can add three bits and get the output in the form of a Sum and a Carry. The truth table for a full adder is given in Table 3.3.

Table 3.3: Truth table of a Full Adder

A	B	C	Carry	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

The inputs are A, B and C, while the outputs are Sum and Carry. You can obtain the Boolean expressions for sum and carry using the sum of products method given in the following:

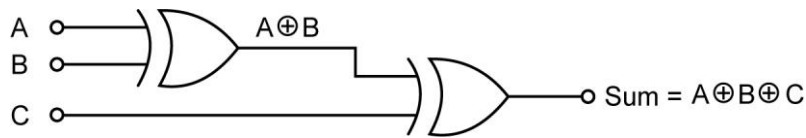
$$\begin{aligned}
 \text{Sum} &= \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC \\
 &= \bar{A}\bar{B}C + \bar{C}(\bar{A}B + A\bar{B}) + ABC = \bar{C}(A \oplus B) + C(\bar{A}\bar{B} + AB) \\
 &= \bar{C}(A \oplus B) + C(\overline{A \oplus B}) \\
 &= \bar{C}x + C\bar{x} \quad (\text{with } x = A \oplus B) \\
 &= x \oplus C \\
 &= A \oplus B \oplus C
 \end{aligned} \tag{3.1}$$

$$\begin{aligned}
 \text{Carry} &= \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC \\
 &= AB(C + \bar{C}) + (\bar{A}B + A\bar{B})C \\
 &= AB + (A \oplus B)C
 \end{aligned} \tag{3.2}$$

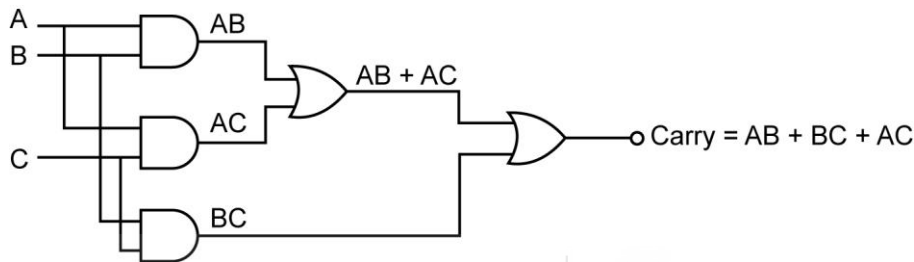
In the theory course, you have learnt that the expression of Carry can also be given by

$$\text{Carry} = AB + BC + CA \tag{3.3}$$

So it is clear that the sum is an XOR operation of A , B and C inputs. This can be achieved by cascading two XOR gates as shown schematically in Fig.3.3a. The carry can be obtained by combination of AND gates and OR gates as shown in Fig. 3.3b.



(a)



(b)

Fig. 3.3: Schematic of a) Sum and b) Carry output of a full adder.

The circuits for sum and carry can be built either by using only NAND gates or basic logic gates. In the following procedure we explain the circuit built using only NAND gates. In consultation with your counsellor you may build the circuits using the basic logic gates as well. In either case you have to build a circuit and obtain its truth table.

Procedure

For building the full adder in total you will require 13 NAND gates that is five NAND gate IC 7400. In Fig. 3.4 the circuit of a full adder using only NAND gates is shown to implement the expressions given by Eq.(3.1) and (3.2).

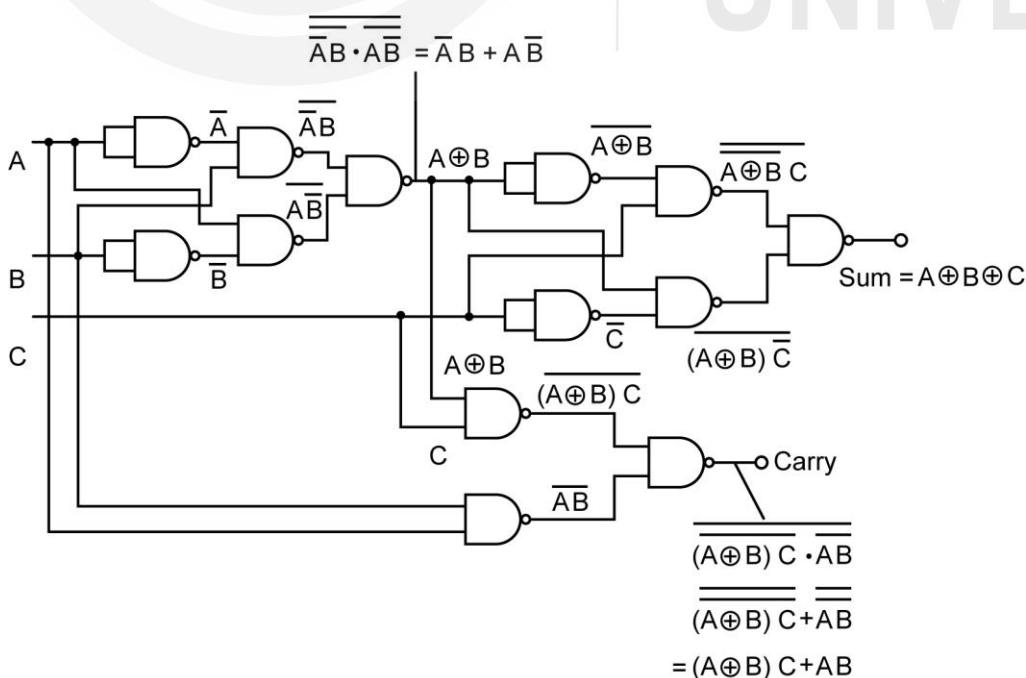


Fig. 3.4: NAND gate circuit of a full adder.

1. Arrange five NAND gate IC 7400 on the breadboard.
2. Give power to all the ICs by connecting pin number 14 to +5V supply. Pin number 7 should be connected to ground.
3. Make the connections of the NAND gates as shown in Fig 3.4.
4. Connect the voltmeter at the output of cascaded chain of NAND gates used for obtaining the Sum output. You can use another voltmeter at the Carry output. If only single voltmeter is available, you can use it for measuring the voltages at both Sum and Carry outputs alternately.
5. Apply the combinations of 0's and 1's to the inputs *A*, *B* and *C* as given in the Observation Table 3.4 and record the corresponding sum and carry voltage readings in each case.

Observation Table 3.4: Truth table of full adder built using NAND gates

<i>A</i>	<i>B</i>	<i>C</i>	Carry	Sum
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

6. Compare to outputs of Sum and Carry recorded by you with the ones given in the truth table in Table 3.3.
7. Report your results and write down the precautions you observed while performing the experiment.

EXPERIMENT 4

DESIGN OF ASTABLE MULTIVIBRATOR USING TIMER IC

Structure

- | | |
|--|--|
| <p>4.1 Introduction
Expected Skills</p> <p>4.2 Timer IC 555 and its Operation</p> <p>4.3 Circuit Familiarisation and Operation as an Astable Multivibrator</p> | <p>4.4 Experimental Set Up
Astable Multivibrator of Variable Frequency with Constant Duty Cycle
Astable Multivibrator of Constant Frequency with Variable Duty Cycle</p> <p>4.5 Further Exploratory Exercise</p> |
|--|--|

4.1 INTRODUCTION

A multivibrator is an electronic circuit that derives its name from the number of stable states that its output terminal has. Such circuits are useful in analogue as well as digital electronics. As you have learnt in Unit 16 of Theory course on Digital and Analog Circuits and instrumentation (BPHET-143), multivibrator circuits fall in three categories – astable, monostable and bi-stable.

An astable multivibrator has no stable state at its output. Once it is powered, the output state keeps alternating between logical 0 and 1 continuously. An astable multivibrator is thus a square wave oscillator that starts from the moment it receives power. The rectangular (square) waveform is predominant in today's world of digital electronics, electronic communication and computers.

A monostable multivibrator can have either 0 or 1 (normally low or high) stable output state. When it receives a momentary trigger, the circuit makes a transition from its stable (quiescent) state to the other state; stays in that state for a predetermined time span and then, on its own, returns to the quiescent state.

A bi-stable can have two output states. Like the monostable multivibrator, it also changes its output state in response to a suitable triggering pulse but it does not return to the previous state on its own. To bring it back to the previous state, another pulse must be externally provided.

To build the astable and monostable multivibrator circuits, timer IC555 has been one of the most popular choices. You will be designing and testing an astable multivibrator using IC 555 in this experiment. You have studied the internal block diagram of IC 555 in Unit 16 of the theory course.

You may recall that, the number 555 is supposed to have been coined due to the three identical $5k\Omega$ resistors in the potential divider configuration to derive reference voltages for the two comparators within the IC. Further, these reference voltages maintain their ratio with each other regardless of the fluctuations in the DC power supplied to the IC. This is the sole reason why the timings of the pulses produced are admirably stable.

Expected Skills

After performing this experiment, you should be able to:

- ❖ construct an astable multivibrator with IC 555 using external passive components so as to produce a rectangular wave with the desired frequency;
- ❖ define the duty cycle of the rectangular waveform; and
- ❖ design a circuit an astable multivibrator circuit to achieve the desired duty cycle.

To perform this experiment you will require following apparatus and components.

Apparatus Required

IC 555, several resistors / potentiometers of desired values to attain required frequency/ duty cycle, capacitors of suitable value, 2 general purpose diodes, dc power supply of +5 to +15 V or a battery of +9 V, CRO, bread board, connecting wires.

4.2 TIMER IC 555 AND ITS OPERATION

You have learnt about the basic blocks of IC 555 in your theory course BPHE-143 working as an astable as well as a monostable multivibrator. As such, we discuss only the aspects which are directly related to the procedural understanding of the experiment here.

Refer Fig.4.1 to know how IC 555 appears.

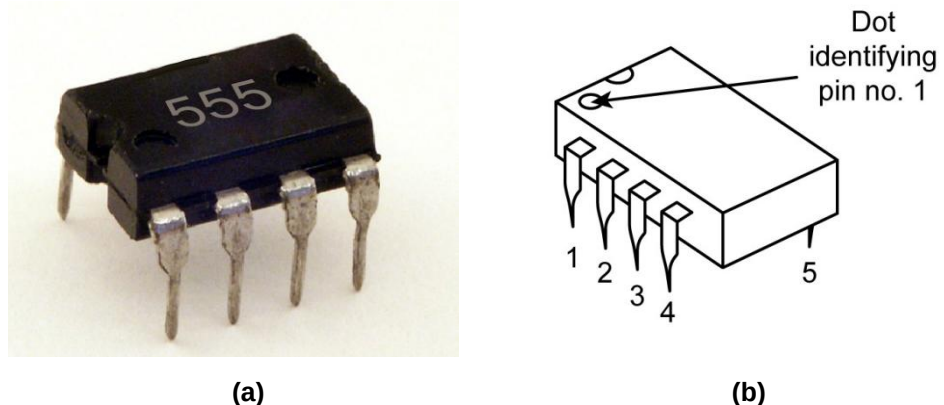


Fig. 4.1: a) Photograph; b) pin identification of dual in line package IC 555.

The pin-out diagram of IC 555 is shown in Fig. 4.2.

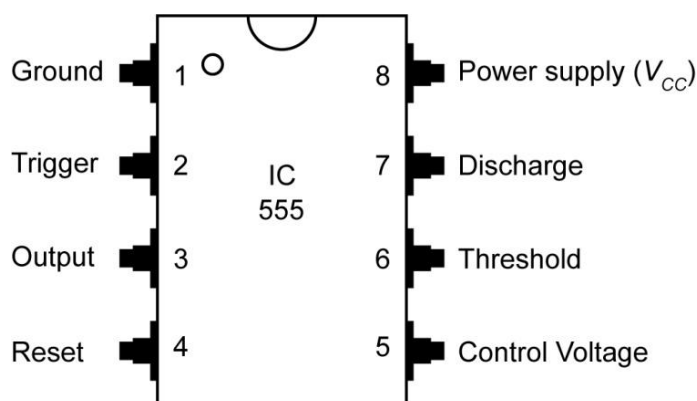


Fig. 4.2: Pin-out diagram of IC 555.

You have studied the functions of all these 8 pins and the block diagram of IC55 in Unit 16 of the theory course BPHET-143. However, for ready reference we reproduce the block diagram here again.

In Fig. 4.3 we have shown a functional block diagram of IC 555.

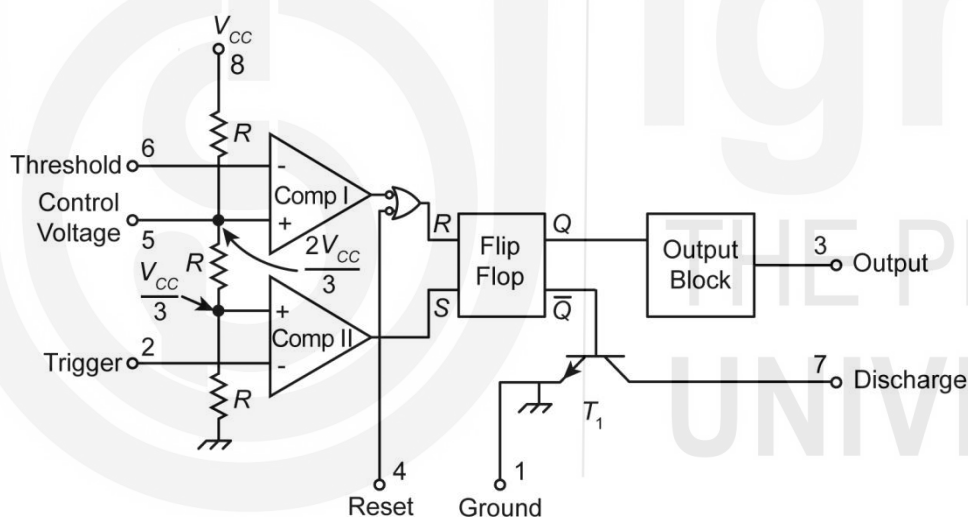


Fig. 4.3: Functional block diagram of IC 555.

There are two comparators: Comparator I and Comparator II. There is a voltage divider in the form of a chain of three equal internal resistors of $5\text{ k}\Omega$ each, connected between the inputs of the two comparators as shown in the figure.

This resistive divider network is used to set the comparator levels. Since all three resistors are of equal value, the threshold comparator (Comp-I) is referenced internally at $2/3$ of supply voltage level and the trigger comparator (Comp-II) is referenced at $1/3$ of supply voltage. The outputs of Comp-I and Comp-II are tied to a flip-flop. The output Q of the flip-flop is used as the output of the IC (pin 3) while $\bar{Q}$, is connected to the base of the discharge transistor T_1 , which operates in its non-linear mode (i.e. it is either cut-off or saturated). With base at low voltage ($\bar{Q} = 0$), it is cut off while with $\bar{Q} = 1$, it is fully ON.

When the trigger voltage is moved below $1/3$ of the supply, the trigger comparator changes state and sets the flop-flop driving the output to a high state. Simultaneously, the transistor T_1 is switched *OFF* and the external timing capacitor starts charging. The threshold pin normally monitors the capacitor voltage of the timing network made of external resistor-capacitor, as will be described in the next sections. When the capacitor voltage exceeds $2/3$ of the supply, the threshold comparator resets the flip-flop which in turn drives the output to a low state. When the output is in a low state, the discharge transistor (T_1) switches *ON*, thereby discharging the external timing capacitor. Once the capacitor is discharged, the timing cycle is completed, and the timer will await for the next trigger pulse.

Now we describe the connections required to build an astable multivibrator using IC555.

4.3 CIRCUIT FAMILIARISATION AND OPERATION AS AN ASTABLE MULTIVIBRATOR

The circuit diagram of an astable multivibrator using IC555 is shown in Fig. 4.4.

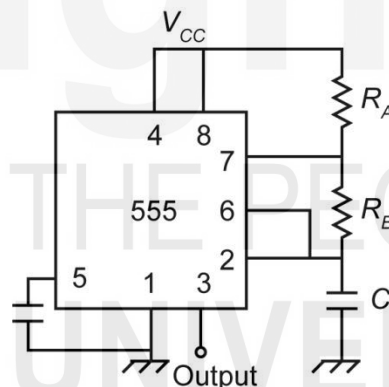


Fig. 4.4: Astable multivibrator.

In the astable (free-run) mode the trigger is tied to the threshold pin. At the time when power is switched on, the capacitor is discharged, holding the trigger low. This triggers the timer, which establishes the capacitor charging path through R_A and R_B . When the capacitor reaches the threshold level of $2V_{CC}/3$ the output drops low and the discharge transistor turns *ON*.

The timing capacitor now discharges through R_B . When the capacitor voltage drops to $V_{CC}/3$, the trigger comparator changes its state, automatically re-triggering the timer, creating a continuously running oscillator circuit.

The waveforms generated by the astable multivibrator at the output pin 3 and across the capacitor (between pin 6 and ground) are shown in Fig. 4.5. (Here we have omitted the first wave cycle just after power on, when capacitor charges from 0 V to $2V_{CC}/3$ V.)

The upper waveform represents the rectangular wave output. You must have noticed that the *ON* time of this rectangular waveform is decided by the

charging time of the capacitor while the *OFF* time is determined by the discharging time of the capacitor.

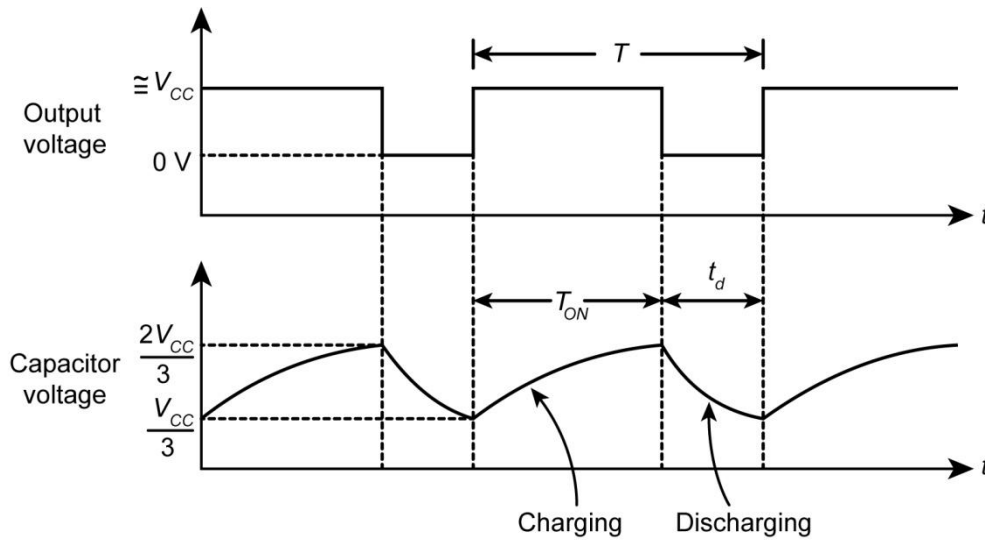


Fig. 4.5: Waveforms of an astable multivibrator.

So the *ON*-time (high) of output is the time taken by the capacitor to charge from $V_{CC}/3$ to $2V_{CC}/3$ through resistors R_A and R_B .

$$\therefore T_{ON} = 0.69(R_A + R_B)C \quad (4.1)$$

where R_A and R_B are in ohms and C is in farads.

Similarly, the *OFF*-time of the waveform is the time taken by the capacitor to discharge from $2V_{CC}/3$ to $V_{CC}/3$ through resistor R_B .

$$\therefore T_{OFF} = 0.69R_B C \quad (4.2)$$

where R_B is in ohms and C is in farads.

Hence the total period of one cycle of the output waveform

$$\begin{aligned} T_{TOTAL} &= T_{ON} + T_{OFF} \\ &= 0.69(R_A + R_B)C + 0.69R_B C \\ &= 0.69(R_A + 2R_B)C \end{aligned} \quad (4.3)$$

The frequency of this rectangular wave oscillator is

$$\begin{aligned} f &= \frac{1}{T_{TOTAL}} = \frac{1}{0.69(R_A + 2R_B)C} \\ &= \frac{1.45}{(R_A + 2R_B)C} \end{aligned} \quad (4.4)$$

Now, when we characterize a rectangular waveform, along with its frequency, we also specify its **duty cycle**. Duty cycle of a waveform is defined as

$$\text{Duty Cycle} = DC = \frac{T_{ON}}{T_{TOTAL}} = \frac{T_{ON}}{T_{ON} + T_{OFF}} \quad (4.5)$$

Sometimes it is also expressed in percentage as

$$\% \text{Duty Cycle} = \frac{T_{ON}}{T_{TOTAL}} \times 100\% \quad (4.5a)$$

Substituting the values of T_{ON} and T_{TOTAL} from Eqs. (4.1) and (4.3) we get

$$\begin{aligned} \text{Duty Cycle} &= \frac{0.69(R_A + R_B)C}{0.69(R_A + 2R_B)C} \\ &= \frac{R_A + R_B}{R_A + 2R_B} \end{aligned} \quad (4.6)$$

A special case of rectangular waveform is a *square waveform*, when $T_{ON} = T_{OFF}$ or the duty cycle = 50%. You will notice that an almost square waveform (duty cycle = 0.5 or 50%) is available by making R_B much larger than R_A . However, if we wish to have the duty cycle less than 0.5, say 0.1 (= 1/10), then a strange situation arises. In such case R_A must be negative, which is absurd. So the conventional circuit is incapable of producing duty cycles of 0 – 50%.

In order to obtain a train of pulses for which the duty cycle should be less than 50%, one or two diodes that separate the charging path from the discharging path for the timing capacitor C might be used. One such circuit is shown in Fig. 4.6.

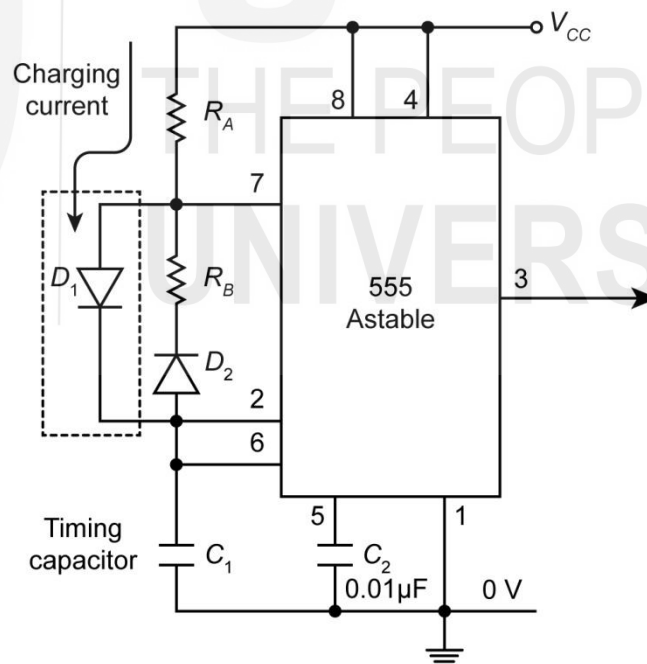


Fig. 4.6: Astable multivibrator circuit to produce duty cycles of less than 50%.

In circuit of Fig. 4.6, the capacitor charges through resistor R_A and diode D_1 whereas the capacitor discharges through the series combination of resistor R_B and diode D_2 . It is usually desirable to use resistors R_A and R_B much larger than the forward-biased diodes dynamic resistance for maintaining the accuracy of timings and to minimise frequency drift due to temperature variation. With this assumption, neglecting the forward resistance of the diodes we can write

$$T_{ON} = 0.69R_A C$$

and

$$T_{OFF} = 0.69R_B C$$

$$\therefore T_{TOTAL} = 0.69(R_A + R_B)C \quad (4.7)$$

and

$$\text{Duty Cycle} = \frac{R_A}{R_A + R_B} \quad (4.8)$$

Now with $R_A = R_B$, we can get a square wave (50% duty cycle) and when R_A is smaller than R_B , we can have duty cycle less than 50%.

In this case the frequency of oscillations is given by

$$f = \frac{1}{T_{TOTAL}} = \frac{1.45}{(R_A + R_B)C} \quad (4.9)$$

4.4 EXPERIMENTAL SET UP

The circuit of an astable multivibrator can be conveniently assembled on a general purpose PCB or a breadboard, although using a printed circuit board tailor-made as per the circuit is a better option that avoids inadvertently made loose connections, which affect the functionality. Since you should measure not only the frequency but also the duty cycle of the waveform, an oscilloscope would be required. The power supply to IC 555 could be anywhere between 5 volts to 15 volts and the use of a 9V DC battery cell would be convenient as it would provide a ripple-free DC to the circuit. It would be a good idea to use a series combination of resistors with potentiometers as the timing resistors for observing how the waveform contracts or expands within safe limits set by the fixed value resistors R_A and R_B of Figs. 4.4 and Fig. 4.6.

You will carry out this experiment in two parts. In the first part, you should take at least 10 different observations of frequencies keeping the duty cycle constant and in the next part, at least five different duty cycles keeping the frequency constant.

4.4.1 Astable Multivibrator of Variable Frequency with Constant Duty Cycle

Suppose you decide to create a set of frequencies with all 50% duty cycle. This would mean that you wish to have $T_{ON} = T_{OFF}$. Using the circuit of Fig. 4.4, you must make R_A much smaller than R_B . Then alone, you can have almost equal ON and OFF timings. To vary the frequency widely, you can adjust the value of R_B alone; say from 25 times that of R_A to 100 times R_A .

If you use the circuit of Fig. 4.6 you do not have this limitation. However, it would be easier if you decide the values of frequencies in advance and calculate the value of $R_A = R_B$ for every frequency desired using Eq. (4.9). Usually the value of the timing capacitor should be about $0.01 \mu\text{F}$ for covering a wide range. Avoid using an electrolytic capacitor (value $1 \mu\text{F}$ or more.)

Build the circuit as shown in Fig. 4.6. Using a breadboard will facilitate changing of the components for every desired frequency. Connect the output (pin 3) to the CRO for observing the output waveform.

For every combination of $R_A = R_B$, record the readings of time period as observed on the CRO screen. Also record the *ON* and *OFF* times of pulses in every case in Observation Table 4.1. Also record the expected frequency calculated from the values of R 's and C .

Observation Table 4.1: Variable frequency with constant duty cycle

Sl. No.	$R_A = R_B$ (Ω)	C (μF)	On time $t_1(\mu\text{s})$	Off time $t_2(\mu\text{s})$	Periodic time (t_1+t_2) = T (μs)	Duty Cycle = t_1/T	Observed Frequency $F_{obs} = 1/T$ (Hz)	Expected Frequency F_{calc} (Hz)
1								
2								
3								
4								
5								
..								
10								

You can determine the error due to component tolerances and personal error in measurement by calculating the difference between the calculated (expected) and observed values of frequency and duty cycles.

Give the reason of the deviation observed in the expected and observed values.

4.4.2 Astable Multivibrator of Constant Frequency with Variable Duty Cycle

In the second part of the experiment, use the circuit shown in Fig. 4.4.

Calculate the values of R_A and R_B using Eq. (4.4) and (4.6) so as to obtain five different duty cycles keeping the frequency constant. As an example, you can keep the frequency constant at 5 kHz and three different duty cycle values of (say) 80%, 70% and 60%. You may consult your Counsellor for deciding the frequency depending on the components available in the laboratory.

Build the circuit of astable multivibrator on a breadboard. Connect the output (pin 3) to a CRO. For every combination of R_A and R_B record the total time period and ON and OFF times of the waveform in Observation Table 4.2.

Observation Table 4.2: Constant frequency with variable duty cycle

Sr No	R_A (Ω)	R_B (Ω) □	C (μF)	On time t_1 (s)	Off time t_2 (s)	Period ($t_1 + t_2$) = T (s)	Duty Cycle = t_1/T	Observed Freq $F_{obs} = 1/T$ (Hz)	Expected Freq F_{calc} (Hz)	Expected Duty Cycle
1										
2										
3										

You can determine the error due to component tolerances and personal error in measurement by calculating the difference between the calculated (expected) and observed values of frequency and duty cycles.

Give the reason of the deviation observed in the expected and observed values.

4.5 FURTHER EXPLORATORY EXERCISE

IC 555 is one of the most popular and widely used timer IC. You may try listing a variety of its succeeding versions and the advantages they offer. Further, you may also attempt to make a list of some important applications wherein the timer is used as an astable multivibrator.

If your mind is inquisitive, you might also like dwelling upon the circuit shown in Fig. 4.7. In this circuit, the timing capacitor charges through the combination of series resistors R_A and R_B whereas the capacitor discharges through series resistors R_B and R_C . The circuit is useful for overcoming the limitation

on the duty cycle of conventional 555 circuit as well as the circuit of Fig. 4.6, in which diodes bring in some undesired temperature dependence. Try to know its advantages and limitations as well.

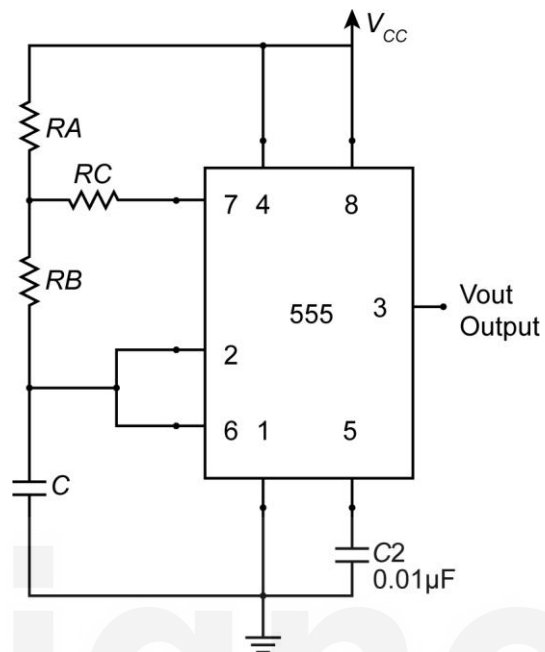


Fig. 4.7: A special circuit to create narrow pulses using IC 555.

EXPERIMENT 5

DESIGN OF MONOSTABLE MULTIVIBRATOR USING TIMER IC

Structure

5.1	Introduction Expected Skills	5.4	Measurement of Output Pulse Width and Verification of Formula
5.2	Operation of the Timer IC 555 as a Monostable Multivibrator	5.5	Further Exploratory Exercise
5.3	Experimental Set Up		

5.1 INTRODUCTION

You have already got acquainted with timer IC555 and the class of circuits called multivibrators in the last experiment. Let us therefore confine our discussion only to the monostable multivibrator in this experiment. Can you guess any situation where you need a monostable multivibrator? Let us cite one such simple situation. Imagine that in a milk packaging plant, you wish to seal the packet after you have poured say half a litre milk in a plastic pouch. The sealing can be done satisfactorily in 5 seconds using a linear heater. You can meet this requirement by feeding the electric mains supply to the heater which, in turn, could be controlled by a monostable multivibrator. If you give it a momentary control pulse after pouring half a litre milk, its output will change from its quiescent (usually '0') state to '1' and that can activate a relay circuit. The relay circuit would turn the heater *ON* just for 5 seconds and thereafter it would automatically shut since the monostable circuit would return to its stable state, turning the relay off. It is noteworthy that a monostable circuit can provide a very large range of timings with suitable components. Due to this feature, you can find numerous applications of the monostable multivibrators such as timers, missing pulse detectors, bounce-free switches, touch switches, frequency divider, capacitance measurement, pulse-width modulators (PWM), and so on.

In this experiment you will build a monostable multivibrator circuit using IC555, which will produce a pulse of desired time length, when a trigger is applied to it.

Expected Skills

After performing this experiment, you should be able to:

- ❖ calculate the component values to obtain a desired pulse width from the monostable multivibrator;
- ❖ construct a monostable multivibrator using IC555; and
- ❖ produce a rectangular pulse of desired duration using a trigger signal.

To perform this experiment you will require the following apparatus and components.

Apparatus Required

IC555, resistors / potentiometers of desired values to attain required pulse width, capacitors of suitable value, , dc power supply of +5 to +15 V or a battery of +9 V, analog voltmeter, tap key, stop watch, CRO, signal generator for rectangular trigger pulse generation, bread board, connecting wires.

5.2 OPERATION OF THE TIMER IC 555 AS A MONOSTABLE MULTIVIBRATOR

We discuss only the aspects which are directly related to your procedural understanding of the experiment here, since you have gained adequate knowledge about the timer IC in the previous experiment.

The configuration required to build a monostable multivibrator is shown in Fig. 5.1.

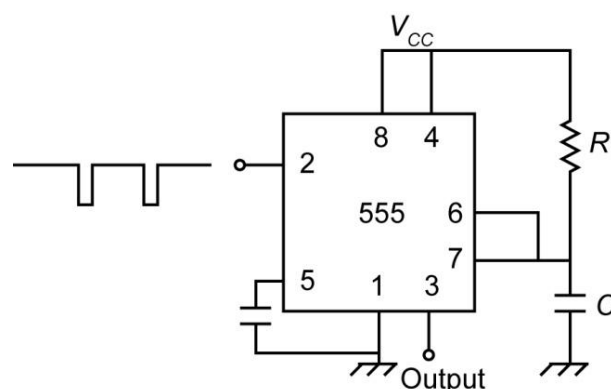


Fig. 5.1: Monostable multivibrator.

The sequence of events starts when a voltage below $V_{CC} / 3$ is sensed by the trigger comparator (Comp-II). The trigger is normally applied in the form of a short negative-going pulse. On the negative-going edge of the pulse, the

device triggers, the output goes high and the discharge transistor turns *OFF*. Note that prior to the input trigger pulse, the discharge transistor is *ON*, shorting the timing capacitor to ground. After trigger action, the timing capacitor, C starts charging through the timing resistor, R' . The voltage on the capacitor increases exponentially with a time constant $T = R'C$. Ignoring capacitor leakage, the capacitor will reach the $2V_{CC}/3$ level in 1.1 times the time constants or

$$t_p = 1.1R'C \quad (5.1)$$

where t_p is in seconds, R' is in ohms, and C is in farads. This voltage level changes the output state of the threshold comparator (Comp-I), which in turn drives the output of the flip-flop low and turns the discharge transistor *ON*. The transistor discharges the capacitor C rapidly. The timer has completed its cycle and will now await another trigger pulse.

Fig. 5.2 shows the waveforms of the monostable operation. The top most waveform is the trigger pulse input given to pin 2. Once the trigger pulse is applied Comp-II sets the flip-flop output (pin 3) to high state. Its voltage goes from 0 to V_{CC} volts. Simultaneously the discharge transistor T_1 switches *OFF* and the capacitor starts charging with $R'C$ time constant. Initially the capacitor is fully discharged; hence it begins to charge from 0 V. It keeps on charging till the threshold comparator (Comp-I) changes its state. This happens when the capacitor voltage is $2V_{CC}/3$. At this moment the flip-flop is reset, output (pin 3) is at 0 V and transistor T_1 turns *ON*. This causes instant discharging of the capacitor to 0V.

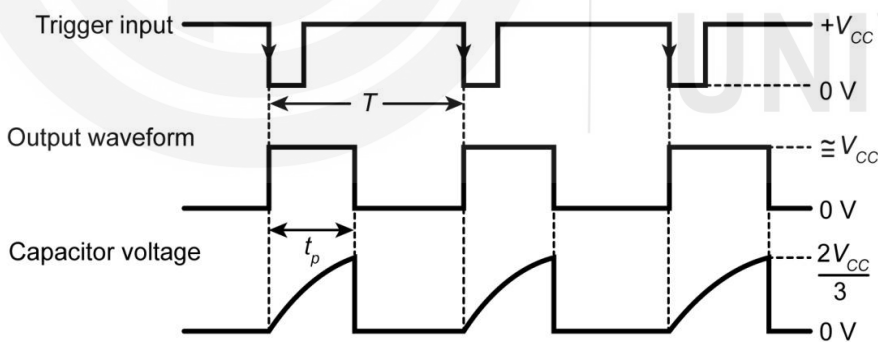


Fig. 5.2: Waveforms of a monostable multivibrator.

In this way we generate a pulse of width t_p at the output of the IC. This pulse width is determined by the relation given by Eq. (5.1).

It is worth noting that the trigger pulse has to be always shorter as compared to the desired duration, which is $t_p = 1.1R'C$. Another pulse given to pin 2 while the output at pin 3 is high, makes no difference; however if the triggering pulse is wider than the duration $1.1R'C$, the output pulse would not end as expected.

5.3 EXPERIMENTAL SET UP

The circuit of a monostable multivibrator can be conveniently assembled on a general purpose PCB or a breadboard, although using a printed circuit board tailor-made as per the circuit is a better option that avoids inadvertently made loose connections, which affect the functionality. As in the previous experiment, the power supply to IC 555 could be anywhere between 5 volts to 15 volts and the use of a 9V DC battery cell would be convenient as it would provide a ripple-free DC to the circuit.

It would be a good idea to use a series combination of resistors with potentiometer as the timing resistor R' in Fig. 5.1. If you choose a time duration of over a few second using suitable R' and timing capacitor C , you can watch the output of the multivibrator going high and returning to the zero state even without an oscilloscope just by using an analog multimeter. In such a case, you can just connect a tap key between terminal 2 of IC555 and ground to provide a short duration manual trigger pulse.

However, if you wish to watch a pulse train at the output, you must connect the output of a rectangular wave signal generator to terminal 2 and adjust its frequency as well as duty cycle properly. In this case, the pulse duration of the monostable output (t_p) could be much shorter than a second (ms or μ s). Ensure that the off time of the square is shorter than the desired pulse duration available at the output (terminal 3) connected to the oscilloscope.

You should note that a continuous variation of the pulse duration available using a potentiometer in series with a fixed low value resistor is an attractive option, but the measurement of the actual value of R' is somewhat tricky. It requires a disconnection of either end of a potentiometer and switching off the dc power supply before you could use a multimeter to measure the resistance of the potentiometer in a particular setting.

As far as possible, avoid using an electrolytic capacitor since the type is known for its wide tolerance which results into large deviation from the printed values of capacitance. Because of this the expected and observed values of output pulse width might differ significantly. If you still insist for a timing of few seconds, you might use a tantalum capacitor safely.

5.4 MEASUREMENT OF OUTPUT PULSE WIDTH AND VERIFICATION OF FORMULA

You can easily perform the experiment by following the simple plan of observations presented in Observation Table 5.1. Remember that the values of resistors are usually quoted in $k\Omega$ whereas those of capacitors in μ F as a convention. You must observe due care regarding units taken to calculate expected pulse duration in micro/milliseconds or even seconds.

Procedure

1. Connect the circuit as shown in Fig. 5.1.

2. If you are studying a long duration pulse, connect the output (pin 3) to an analog multimeter and connect a tap key between the trigger input (pin 2) and ground.
3. If you are studying a short duration pulse width, connect a signal generator to the trigger input. You should choose the rectangular waveform output with very large duty cycle, so that the duration of the low going pulse, acting as the trigger, is short. Simultaneously, connect this waveform to Channel I of the CRO. Connect the output (pin 3) of the multivibrator circuit to Channel II of the CRO.
4. Measure the pulse width at the output of the circuit either with the help of a stop-watch or on CRO, depending upon the pulse width and the trigger frequency.
5. Record your readings of pulse duration for each value R' and C in the Observation Table 5.1.
6. Also record the expected pulse duration calculated using Eq. (5.1) in the table.
7. Calculate the percentage error in the observed and expected pulse duration.
8. Repeat steps 4 to 7 for at least 5 different combinations of R' and C values.

Observation Table 5.1: Monostable multivibrator pulse width

Sl.No.	R' (Ω)	C (μF)	Expected pulse duration $t_{p(exp)} = 1.1R'C$ (s)	Observed pulse duration $t_{p(obs)}$ (s)	% error = $\frac{t_{p(exp)} - t_{p(obs)}}{t_{p(exp)}} \times 100$
1					
2					
3					
4					
5					

Results: Are the expected values of pulse duration matching with the observed ones?

Report the percentage error in your observations.

State the reasons for the deviations observed.

5.5 FURTHER EXPLORATORY EXERCISE

IC 555 is one of the most popular and widely used timer IC. You may try listing a variety of its succeeding versions and the advantages they offer. Further, you may also attempt making a list of some important applications wherein the timer works as a monostable multivibrator.

If your mind is inquisitive, you might also like dwelling upon a complementary circuit. Such a circuit should have logical level 1 as its quiescent state. On providing an external pulse (where?), the circuit should make a transition to 0 (zero) state and after the predetermined duration, must revert to its quiescent state. The important condition is that such a basic configuration (circuit) must not employ any external transistor as inverter.



EXPERIMENT 6

STUDY OF I - V CHARACTERISTICS OF SPECIAL DIODES (ZENER AND LED)

Structure

- 6.1 Introduction
 - Expected Skills
- 6.2 Zener Diode
 - Working of a Zener Diode
 - I - V Characteristics of a Zener Diode

- 6.3 I - V Characteristics of a Light Emitting Diode

6.1 INTRODUCTION

In Unit 2 of the theory course on Digital and Analog Circuits and Instrumentation (BPHE-143) you have got introduced to the semiconductor junction diodes. You will recall that materials can be broadly classified into conductors, insulators and semiconductors on the basis of their resistivity. The resistivity of a conductor is of the order of $10^{-7} \Omega\text{m}$ and that of an insulator is of the order of $10^{12} - 10^{24} \Omega\text{m}$. The resistivity of a semiconductor lies in-between the resistivities of a conductor and an insulator. Germanium (Ge) and Silicon (Si) are the most commonly used semiconductors. At absolute zero, the semiconductor also acts as a near perfect insulator. But with increase in temperature, the conductivity of the semiconductor increases. This change in conductivity with temperature is different for different semiconducting materials. The conductivity of a semiconductor can also be influenced by doping it with some impurity elements, called **dopants** like boron, phosphorus, arsenic etc. Depending on the type of carrier added by a dopant, the semiconductor is classified as p -type (hole carriers) or n -type (electron carriers). The p -type impurity is acceptor type, whereas the n -type impurity is donor type.

When the anode is connected to +ve terminal of battery and the cathode is connected to -ve terminal of the battery, the device is said to be *forward biased* and when the anode is connected to -ve terminal of battery and the cathode is connected to +ve terminal of the battery, the device is said to be *reverse biased*.

A *p-n* junction is usually formed by doping a part of a pure semiconductor with acceptor impurities and the remainder with donor impurities. Semiconductors have very useful properties (small size, light weight and efficient operation) and are being extensively used in electronic equipments. You may recall that microelectronic chips are the cores of computers and these are also made using semiconductor junctions. Now this limit has been extended to nano-electronic devices.

A *p-n* junction is called a **diode**. There are various types of diodes. You have performed Experiment 9 in the laboratory course on Electricity and Magnetism (BPHCL-134) for plotting and interpreting the *I-V* characteristics of a *p-n* junction diode used in rectifier circuits.

In this experiment, you will draw the *I-V* characteristic curves of some special *p-n junction* diodes like *Zener Diode* and *Light Emitting Diode (LED)*. You have learnt in Unit-2 of the theory course that these diodes can be fabricated by proper doping of the semiconductor.

Both of these diodes are used for different applications: Zener diode is used as a constant voltage reference in the regulated power supply circuits as discussed in Unit 12 of the theory course BPHET-143. The LEDs are a popular source of light in vehicles, home-lighting and as indicator lamps on various instruments and gadgets. In this experiment you will build the circuits to measure the forward and reverse characteristics zener diode and the forward characteristics of LEDs of different colours.

Expected Skills

After performing this experiment, you should be able to:

- ❖ assemble the circuits to bias a zener diode in forward and reverse conditions;
- ❖ plot the forward and reverse bias *I-V* characteristics of a zener diode and determine its breakdown voltage;
- ❖ assemble the circuit to forward bias a light emitting diode; and
- ❖ plot the forward *I-V* characteristics of an LED and determine its knee voltage.

You will require the following components and equipments to perform the experiment.

Apparatus Required

The kits to measure the *I-V* characteristics of zener diode and LEDs

OR

A zener diode, light emitting diodes (LED) of 2-3 different colours, a variable power supply (0-15 V), a dc voltmeter, a milliammeter (0-50mA), a resistance box, breadboard, connecting wires.

6.2 ZENER DIODE

In Sec.2.3.1 of Unit 2 of the theory course BPHET-143 you have learnt about the zener diode, however for brevity, we recapitulate the important features of zener diode here. You know that zener diode allows current to flow not only in the forward direction like a rectifying diode, but also in the reverse direction, when the voltage is more than the breakdown voltage. This voltage is also called **Zener voltage**.

6.2.1 Working of a Zener Diode

The *p*- and *n*- regions in a zener diode are heavily doped. These result in a very thin depletion layer, due to availability of a large number of carriers for recombination near the junction. However, the minority carriers present in the diode as a result of thermal excitations cannot cross the junction due to its barrier potential. When a reverse bias is applied, a large electric field is established across the junction. This field (i) accelerates the already available minority carriers, which, in turn, collide with the atoms of the semiconductor material and eject more electrons through energy transfer (*avalanche effect*) and (ii) breaks covalent bonds resulting in creation of additional electron-hole pairs in the junction region (zener effect). Both these processes give rise to large reverse current even for a small increase in reverse bias voltage. This process is termed as *zener breakdown*. However, since the (magnitude of) reverse voltage is small, the junction is not damaged. In silicon diodes, Zener effect dominates up to about 5.6 V, and beyond this, avalanche effect prevails. The symbol of zener diode is shown in Fig. 6.1.

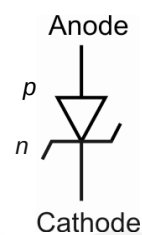


Fig. 6.1: Symbol of zener diode.

6.2.2 *I-V* Characteristics of a Zener Diode

A typical *I-V* characteristic plot of a zener diode is shown in Fig. 6.2. The reverse breakdown voltage is indicated by V_z . The Zener breakdown voltage (V_z) is of great significance in the operation of Zener diode as a voltage regulator.

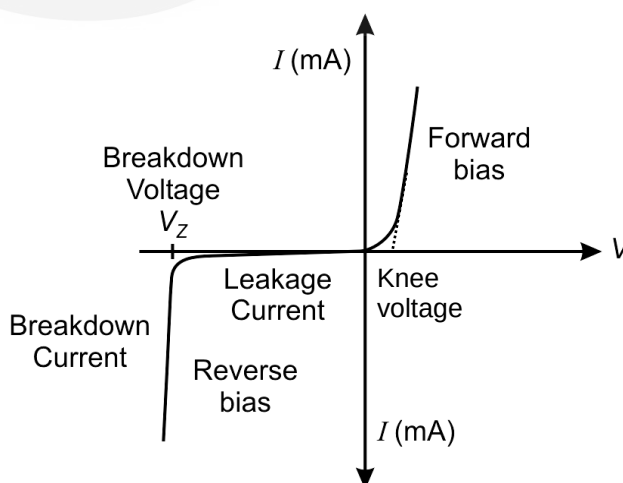


Fig. 6.2: *I-V* characteristics of a zener diode.

You now know that Zener diode can sustain a constant voltage across it in reverse breakdown condition. For this reason, it is always used as a voltage reference in reverse bias. Since resistance in breakdown region is very small,

the current through the diode has to be limited by varying the resistance in the circuit. The value of resistor is chosen in such a way that the product of zener breakdown voltage and reverse current through the zener, i.e. the power dissipated across the junction, is within the power handling capability of the diode. If this limit is exceeded, a large current may damage the diode.

The circuit to study forward I - V characteristics of zener diode is shown in Fig. 6.3a. In this circuit, the value of resistor R is determined by the power rating of the zener diode. The maximum current flowing through R should be less than the diode current rating I_Z .

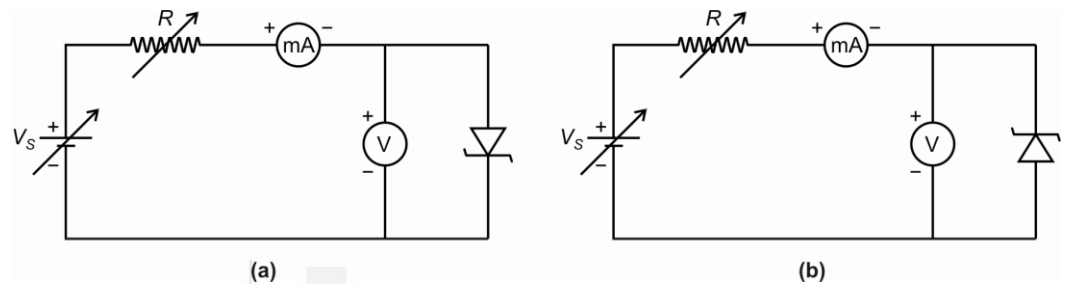


Fig. 6.3: Circuit diagram to determine I - V characteristics of zener diode in a) forward bias; and b) reverse bias.

Take a variable dc voltage supply V_s in the range 0-15V. If the zener breakdown voltage (V_Z) is 10V and maximum current rating (I_Z), is 100 mA, the value of R is given by

$$R = \frac{V_{max} - V_Z}{I_Z} = \frac{(15 - 10) \text{ V}}{100 \text{ mA}} = 50 \, \Omega.$$

Procedure:

1. First check that the junction is working properly using a multimeter.
2. Next make a circuit as shown in the Fig. 6.3a for forward bias I - V characteristics.
3. V_s is a variable power supply. Keep the voltage control in the minimum position and switch on the power supply.
4. Increase the voltage in steps of 0.1V and note the corresponding values of current until an appreciable deflection is observed in the milliammeter. You will note that current in the circuit is small as long as the applied voltage is less than the barrier potential. Once this potential is crossed, the current will increase rapidly with small increase in voltage. The forward voltage required to get the junction in conduction mode is called **knee voltage**. Beyond knee voltage, current increases rapidly.
5. Record your readings in Observation Table 6.1. Note that in no case, you should exceed the maximum forward current rating of the diode in forward bias condition.
6. Next decrease the voltage in same steps and note down the corresponding current values. Record these current and voltage values also in Observation Table 6.1. Are the values of current same in both cases? Calculate the mean value of current for each value of V .

Observation Table 6.1: Forward biased zener diode characteristics

S.No.	Forward Voltage (V)	Forward Current (mA)		Mean Forward Current (mA)
		Increasing voltage	Decreasing voltage	
1.	0.0			
2.	0.1			
3.	0.2			
4.	0.3			
.	.			
.	.			

7. Now reverse the Zener diode bias by connecting the cathode to the positive end and the anode to the negative end of supply. This configuration is shown in Fig. 6.3b. Note that here also, you have to use a milliammeter.
8. Start the power supply from zero volt and increase voltage in steps of 0.5V. Note down the voltage across the Zener diode and the corresponding current flowing through the circuit.
9. Record your readings in Observation Table 6.2.
10. Plot forward and reverse bias *I-V* characteristic curves of Zener diode. Do your curves resemble the *I-V* characteristics shown in Fig. 6.2?

Observation Table 6.2: Reverse bias *I-V* characteristic of a Zener diode

S. No.	Reverse Voltage (V)	Reverse Current (mA)		Mean Reverse Current (mA)
		When increasing Voltage	When decreasing Voltage	
1.	0.0			
2.	0.5			
3.	1.0			
.	.			
.	.			
.	.			

Result: Knee-voltage = ...V

Forward Resistance = ... Ω

Break down Voltage = ...V

Reverse resistance = ... Ω

After performing the experiment on the zener diode, now you should study the characteristics of the light emitting diodes.

6.3 *I-V* CHARACTERISTICS OF A LIGHT EMITTING DIODE

Table 6.3: Some typical LED materials that give rise to different colours (wave lengths in nm)

LED material	Colour
Gallium Phosphide (610 – 760)	Red
Gallium Arsenide Phosphide (570-590)	Yellow
Gallium Indium Phosphide (500-570)	Green
Indium gallium Nitride (400-450)	Violet

An LED or light emitting diode is a *p-n* junction diode that emits light when it is **forward biased**. LEDs are constructed using heavily doped *p-n* junction diodes made of special compounds of semiconductors. Due to heavy doping, the depletion region in LEDs is very thin. Electrons and holes recombine in the junction region and emit light because these materials have direct band gaps suitable for light emission. Some of these materials are listed in Table 6.3, along with the colours of the light produced by them.

You have learnt about generation and recombination of electron-hole pairs in semiconductors and *p-n* junction diodes. The energy of photons in the visible region corresponds to 2 to 3 eV.

In *p-n* junction diodes made of materials like gallium arsenide phosphide (GaAsP) and gallium phosphide (GaP) that have *direct band gap*, energy is emitted in the form of light (rather than heat) when electron-hole pairs recombine in the thin junction region. By suitable doping of semiconducting materials like gallium arsenide, phosphorus, LEDs that radiate red, green, yellow, orange, violet light or infrared radiation can be produced. You may have seen these colours in strings of LEDs in festival lights.

The circuit symbol of an LED is shown in Figs. 6.4a. Like all junction diodes, LED also has an anode and a cathode terminal. Typical LEDs are shown in the photo given in Fig. 6.4b. You will observe that the two leads (terminals) of the LED are of unequal lengths. The longer lead indicates the anode and the shorter one the cathode.

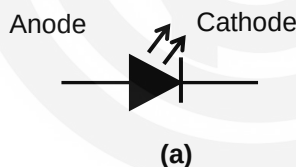


Fig. 6.4: a) Symbol; b) photograph of LED.

LED is basically a **forward biased** *p-n* junction diode in which the depletion region width and the resulting potential barrier across the junction are reduced. Electrons from the *n*-type region and holes from the *p*-type region flow more readily across the junction into the opposite type region. Thus, minority charge carriers are effectively injected across the junction by the application of the external voltage and a current is formed. The increased concentration of minority charge carriers in the opposite type region in the forward biased LED leads to recombination of charge carriers across the band gap along with the emission of energy in the form of a photon.

You must remember that **LED is operated only in the forward bias, and never in reverse bias. If operated in reverse bias, LED can get damaged.**

To measure the *I-V* characteristics of an LED build a forward biasing circuit as shown in Fig. 6.5.

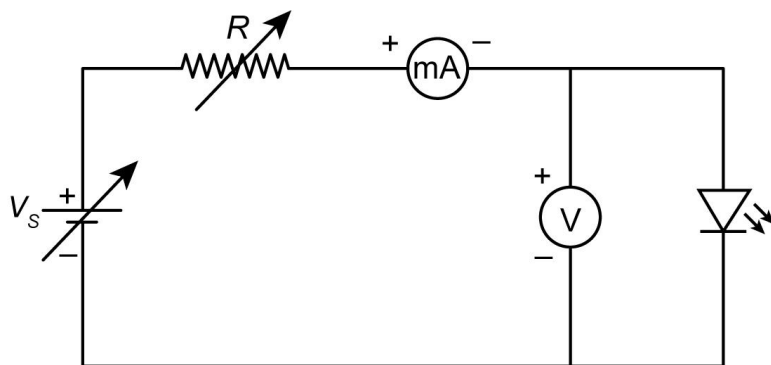


Fig. 6.5: Circuit to measure forward bias I - V characteristics of LED.

Following the similar procedure as used for forward biased zener diode, measure the I - V characteristics of an LED and record the voltage and current readings in Observation Table 6.4. You can take the voltage increment in the steps of 0.2 V.

You will notice that initially, the current is quite low and the LED does not glow. However, as voltage increases, slowly the current starts increasing, and simultaneously the LED starts glowing. In the observation table you should also record the brightness of the LED in terms like no glow, deem, medium bright, brighter etc.

Observation Table 6.4: Forward biased LED characteristics

Colour of the LED under study :

S.No.	Forward Voltage (V)	Forward Current (mA)		Mean Forward Current (mA)	Brightness of LED
		Increasing voltage	Decreasing voltage		
1.	0.0				
2.	0.2				
3.	0.4				
4.	0.6				
.	.				
.	.				

Now take another LED of different colour and connect in the circuit and measure its I - V characteristics. Note down the readings in an Observation Table that you will prepare on your own.

Repeat this procedure for one more colour LED, if available.

Plot the forward bias I - V graphs of all the LEDs on the same graph paper.

Determine the knee voltage for each colour LED and report it under the results. Compare their knee voltages with the knee voltage of the zener diode measured in the first part of the experiment.

Results

LED Number	LED Colour	Knee Voltage
1		
2		
3		
Zener Diode	-----	

Precautions

1. Identify the anode and cathode terminals of the diode properly.
2. Carefully connect the circuits for forward and reverse bias readings of the zener diode.
3. Ensure that you use proper value of resistor in the circuits, so that the current in the diode does not exceed its maximum specified limit.
4. Connect the LED ONLY in FORWARD BIAS condition.

EXPERIMENT 7

STUDY OF TRANSISTOR CHARACTERISTICS IN *CE* MODE AND DESIGN OF *CE* AMPLIFIER

Structure

7.1	Introduction Expected Skills	7.5	Design of <i>CE</i> Amplifier Biasing the BJT Amplifier Circuit Determining the Circuit Elements for a Universal Bias Arrangement Gain and Frequency Response of an Amplifier
7.2	Recapitulation of Transistor Essentials Transistor Configurations		
7.3	Identification of Terminals of a Transistor		
7.4	Transistor Characteristics in <i>CE</i> -Configuration Input Characteristics Output Characteristics Transfer Characteristics		Appendix 7A: Some Common Transistor Packages

7.1 INTRODUCTION

In the preceding experiment, you learnt to plot the I - V characteristics of a zener diode and LED. A more useful semiconductor device is a bipolar junction transistor (BJT). Transistors find many and varied uses in our daily life ranging from gas lighter and toys to amplifiers, radio sets and televisions. In fact, their use is consistently increasing. In the form of switching device, these can be used to regulate vehicular traffic on the roads. They form key elements in computers, space vehicles, power systems, satellites and communication. In a sense, transistors have brought about a revolution, which has helped upgrade technology and improve efficiency

The transistor derives its name from its action as resistor that transfers charges:
Transfer resistor

The practical use of a semiconductor device in electronic circuits depends on the current and voltage (I - V) relationship, as it gives vital information to a circuit designer as well as a technician. Therefore, the first thing of interest is: How does a transistor respond to voltage applied to it? Is the response linear? In your school physics, you have learnt that for a resistor, the characteristic curve (I - V plot) is a straight line passing through the origin. This is manifestation of Ohm's law. For a p - n junction diode, the characteristic curves are non-linear. In Unit 4 of theory course on Digital and Analog Circuits and Instrumentation (BPHEL-143) you have learnt about the input-output I - V characteristics of the transistor. In this experiment, you will obtain characteristic curves for a transistor in the common-emitter mode and calculate current gain, input resistance and output admittance.

The most common application of the transistor is in the amplifier circuits. Therefore, it is apt that you should study a basic amplifier circuit. You will also learn to design a common-emitter amplifier and test its performance.

Expected Skills

After performing this experiment, you should be able to:

- ❖ study variation of base current with potential difference between the base and the emitter (input characteristics) in common-emitter (CE) configuration;
- ❖ study variation of collector current with potential difference between the collector and the emitter (output characteristics) in CE -configuration;
- ❖ examine the relationship between collector current and base current (transfer characteristics) in CE -configuration;
- ❖ calculate current gain, input resistance and output admittance from the characteristic curves;
- ❖ draw the circuit of CE amplifier in universal bias configuration;
- ❖ set up an RC coupled audio frequency amplifier in the common emitter configuration; and
- ❖ determine the voltage amplification factor of the amplifier.

You will require following apparatus for performing this experiment.

Apparatus Required

For transistor characteristics:

Two low range (0-3V and 0-15V) variable dc power supplies, a multimeter, a multi-range microammeter (up to 100 μ A), two multi-range milliammeters (100mA), two multi-range voltmeters, a BC107 n - p - n transistor (or any other n - p - n transistor) with a socket, two 2.5 k Ω /2W potentiometers, one (500-1000) Ω variable resistor and connecting wires, breadboard or transistor characteristic kit.

For Common Emitter amplifier design:

BJT (audio frequency n - p - n transistor), $\frac{1}{2}$ W resistors of chosen values – 4 nos, 10 μ F (>16V) electrolytic capacitor–3 nos, signal generator, CRO, dc power supply, breadboard and connecting wires.

7.2 RECAPITULATION OF TRANSISTOR ESSENTIALS

In Unit 3 and 4 of the theory course BPHET-143 you have studied the basics of transistor like its construction and working. In those units you have got familiarized with the following essential parameters of the transistor.

The *dc alpha* of a transistor indicates how close collector current (I_C) and emitter current (I_E) are. It is defined as

$$\alpha_{dc} = \frac{I_C}{I_E} \quad (7.1)$$

This dc alpha is also referred to as *large signal current gain*. You know that the value of α_{dc} is nearly equal to but always less than one.

Similarly, we can relate the collector current to the base current. It is referred to as *dc beta* of a transistor:

$$\beta_{dc} = \frac{I_C}{I_B} \quad (7.2)$$

Beta signifies the current gain of the transistor in common-emitter configuration. Value of β_{dc} is considerably larger than one.

Since emitter current is sum of collector current and the base current, we can write

$$I_E = I_C + I_B$$

or

$$\frac{I_E}{I_C} = 1 + \frac{I_B}{I_C} \quad (7.3)$$

In terms of α_{dc} and β_{dc} , we can rewrite it as

$$\frac{1}{\alpha_{dc}} = 1 + \frac{1}{\beta_{dc}}$$

or

$$\beta_{dc} = \frac{\alpha_{dc}}{1 - \alpha_{dc}} \quad (7.4)$$

In the theory course, you have also got familiar with the different ways in which a transistor is configured in a circuit.

7.2.1 Transistor Configurations

A transistor is a two-port device. It can take an input and deliver an output. For both input and output, two terminals are needed. This can be done in a transistor by making one of the three terminals common. The configurations of a transistor in which one of the terminals is common to both input and output are shown in Fig. 7.1:

- i) when emitter is common to both input and output circuits, we obtain common emitter (CE) configuration (Fig. 7.1a);

- ii) when base is common to both input and output circuits, we obtain common base (CB) configuration (Fig. 7.1b); and
- iii) when collector is common to both input and output circuits, we have common collector (CC) configuration (Fig. 7.1c).

In each of these configurations, the transistor characteristics are unique. The CE configuration is used most widely because it provides voltage, current and power gains. In the CB configuration, the transistor can be used as a constant current source while the CC configuration is frequently used for impedance matching.

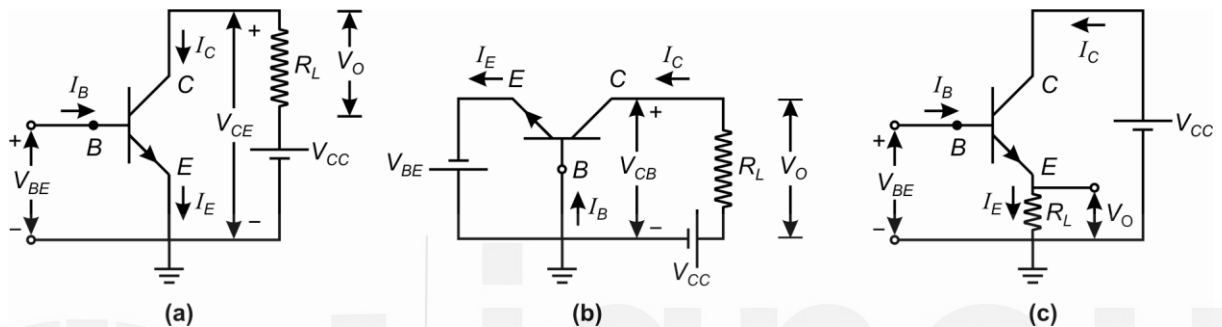


Fig. 7.1: Transistor configuration a) CE; b) CB; c) CC.

For each configuration, we can plot three different characteristics: a) **input characteristics**; b) **output characteristics**; and c) **transfer characteristics**, depending on the nature of quantities involved.

Table 7.1 gives various quantities related to each of these characteristics in all the three configurations and the transistor constants of interest.

Table 7.1: Physical quantities of interest in different characteristics of a transistor

Configuration	Input characteristic	Output characteristic	Transfer characteristic	Important transistor constant
CE	V_{BE} and I_B with V_{CE} as parameter	V_{CE} and I_C with I_B as parameter	I_B and I_C	Current gain, β
CB	V_{BE} and I_E with V_{CB} as parameter	V_{CB} and I_C with I_E as parameter	I_E and I_C	Large signal current gain, α
CC	V_{CB} and I_B with V_{CE} as parameter	V_{CE} and I_E with I_B as parameter	I_B and I_E	

Before you start the experiment, it is essential for you to know to differentiate the base, emitter and collector leads of the given transistor. You will now learn to identify the three terminals of a transistor.

7.3 IDENTIFICATION OF TERMINALS OF A TRANSISTOR

A transistor is usually enclosed in a metal cap. It radiates to the surroundings whatever heat is generated due to flow of electrons. A small notch is provided on this cap and the *terminal close to the notch is emitter*. To identify other two terminals, turn the transistor up-side-down. By referring to Fig. 7.2, you can easily identify the base and the collector. (Some other packages of transistors are shown in Appendix 7A)

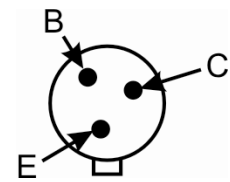


Fig. 7.2: Identifying transistor leads from bottom view.

In a digital multimeter, usually a slot is provided to measure β -value of the transistor. By inserting the transistor in this slot, its β -value is displayed on the panel of the digital multimeter. Usually β ranges from 50 to 150 and depending on the application, a transistor of proper β value can be chosen. The commonly used transistors like BC107 and BC108 are *n-p-n* transistors with β value around 100.

You may now like to answer an SAQ.

SAQ 1 - Identifying a transistor

How can we distinguish an *n-p-n* transistor from *p-n-p* using a multimeter?

In this experiment you will work with a transistor in the CE configuration.

7.4 TRANSISTOR CHARACTERISTICS IN CE-CONFIGURATION

First of all, identify the emitter, base and collector of the given transistor following the steps given above. Next, check that it is working properly by using a multimeter; that is check that emitter-base and collector-base junctions are in order. Now, follow the procedure given below to obtain the input and output characteristics.

7.4.1 Input Characteristics

1. Make the connections as shown in Fig. 7.3. V_{BB} is a variable dc supply of 0-3V and V_{CC} is a variable dc supply of 0-15V. R_1 and R_2 are 2.5 k Ω /2W potentiometers, and R is a variable resistor.

In case a transistor kit is given to you, ensure that the basic circuit given in Fig. 7.3 is in operation. (If you are given a *p-n-p* transistor, you will have to reverse the polarities of batteries and various meters.) By means of potentiometers R_1 and R_2 , you can adjust the voltage in the base and collector circuits, respectively.

2. Keep collector to emitter voltage (V_{CE}) at zero volt.
3. Change V_{BE} from 0 in steps of 0.1V and observe corresponding base current I_B in μ A. Record your readings in Observation Table 7.2. We expect that so long as $V_{BE} < 0.5$ V, there will be no measurable base current, i.e., $I_B = 0$.

4. When V_{BE} is about 0.5V or 0.6V, there may be a small base current of about 2 μA . With a slight increase in voltage (say, by 0.1V), the base current I_B may begin to rise steeply, say up to 20 μA or more. The voltage should not be increased further.

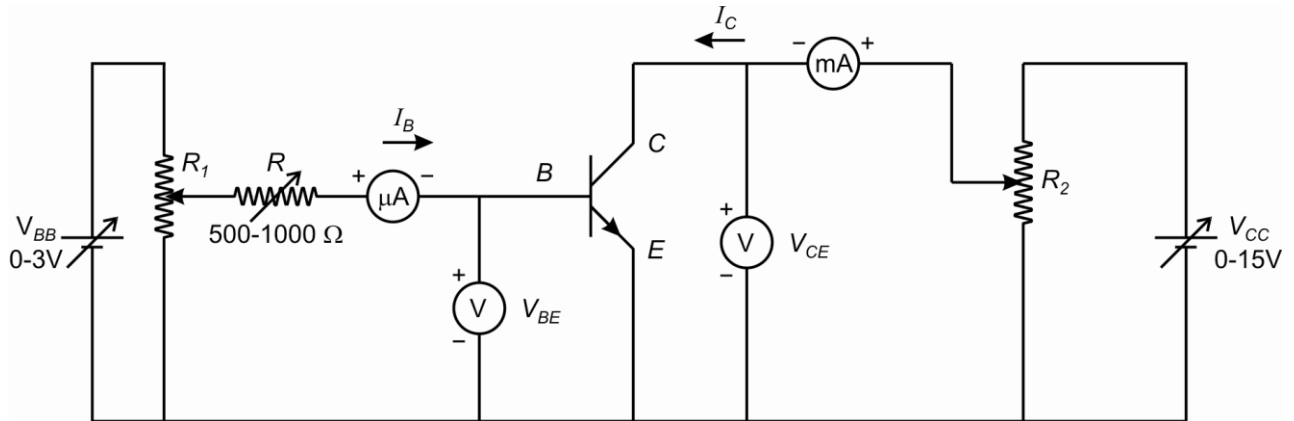


Fig. 7.3: Circuit diagram for determining characteristics of an *n-p-n* transistor in CE-configuration.

5. Repeat steps 3 and 4 for a few values of V_{CE} (say) = 2V, 4V, 6V etc. by varying R_2 . Note that in no case, V_{CE} should exceed 12V.

Observation Table 7.2: Input characteristics of a transistor in CE-mode

V_{BE} (V)	I_B (μA)			
	$V_{CE} = 0$	$V_{CE} = 2\text{V}$	$V_{CE} = 4\text{V}$	$V_{CE} = 6\text{V}$
0.1				
0.2				
0.3				
0.4				
0.5				
0.6				

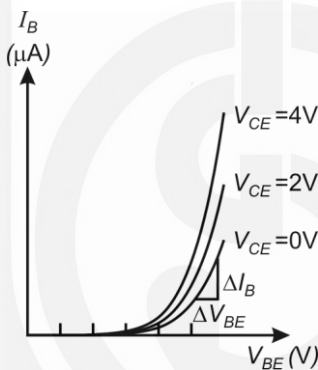


Fig. 7.4: Typical input characteristics of a transistor in CE-mode.

Now plot a graph by taking I_B along the y-axis and V_{BE} along the x-axis for each value of V_{CE} and draw best fit curves, as shown in Fig. 7.4. These are referred to as *input characteristics*. Select a suitable point in the linear portion of the curve and calculate the slope at that point by drawing a tangent. This will give you the value of input resistance, defined as $h_{ie} = \frac{\Delta V_{BE}}{\Delta I_B}$, where ΔV_{BE}

and ΔI_B denote small changes in base to emitter voltage and base current, respectively.

Result: The input resistance h_{ie} for the given transistor is Ω .

7.4.2 Output Characteristics

For obtaining output characteristics also, you should use the circuit shown in Fig. 7.3 and follow the steps given below:

1. Fix the base current I_B at $20\mu\text{A}$ by adjusting R_1 and R .
2. Vary the collector to emitter voltage V_{CE} by varying R_2 from 0 to 10V in steps of 0.5V.
3. Note the collector current I_C in each case and record it in Observation Table 7.3.
4. Repeat steps 2 and 3 for $I_B = 40\mu\text{A}$, $60\mu\text{A}$, and $80\mu\text{A}$. Make sure that you do not exceed the maximum base current rating of the transistor.
5. Plot V_{CE} versus I_C for different values of I_B . Draw smooth curves for each I_B . These are the output characteristics. Typical output characteristics of a transistor are shown in Fig. 7.5.

You can calculate output admittance (h_{oe}) using the relation $h_{oe} = \frac{\Delta I_C}{\Delta V_{CE}}$.

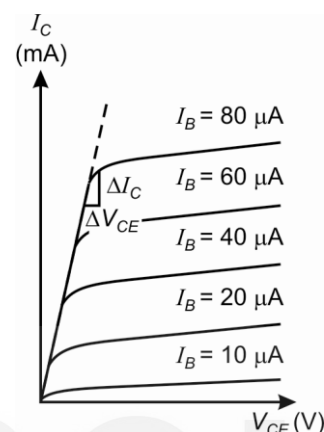


Fig. 7.5: Typical output characteristics of a transistor.

Observation Table 7.3: Output characteristics of a transistor

S.No.	V_{CE} (V)	Collector current I_C (mA)			
		$I_B = 20\mu\text{A}$	$I_B = 40\mu\text{A}$	$I_B = 60\mu\text{A}$	$I_B = 80\mu\text{A}$
1.	0.0				
2.	0.5				
3.	1.0				
.	.				
.	.				

Result: The output admittance for the given transistor is = ... Ω^{-1} .

7.4.3 Transfer Characteristics

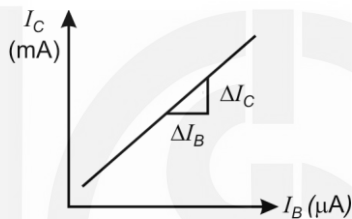
To obtain transfer characteristics, follow the steps given below:

1. Set V_{CE} at 5.0 V.
2. Set the base current I_B at $10\mu\text{A}$ by adjusting R_1 and R . Measure the collector current I_C and record it in Observation Table 7.4.
3. Change the base current to $15\mu\text{A}$. Do you observe any change in V_{CE} ? If yes, then you should adjust R_2 to restore V_{CE} at 5.0V. Again note the collector current.
4. Repeat your observations by increasing I_B in step of $5\mu\text{A}$ till the maximum of $50\mu\text{A}$, keeping V_{CE} constant at 5.0V. You may have to adjust R_2 every time. Record the collector current in Observation Table 7.4.

5. Next fix V_{CE} at 6.0V and repeat steps 2-4.
6. If time permits, you may repeat the above procedure by keeping V_{CE} at 4.0V.
7. Now plot I_B along x-axis and I_C along y-axis for different values of V_{CE} .

Observation Table 7.4: Transfer characteristics of a transistor

S. No.	$I_B (\mu A)$	Collector current I_C (mA)	
		$V_{CE} = 5.0V$	$V_{CE} = 6.0V$
1.	10		
2.	15		
3.	20		
.	.		
.	.		
.	.		
.	.		
.	.		

**Fig. 7.6: Typical transfer characteristic of a transistor in CE-mode.**

Draw a smooth best-fit curve through the observed points. We expect you to get a straight line graph similar to the one shown in Fig. 7.6. Calculate current gain β using the relation

$$\beta = h_{fe} = \frac{\Delta I_C}{\Delta I_B}$$

Result: The current gain for the given transistor is =.....

After obtaining the transistor characteristics in this part of the experiment, now you can perform an experiment to design a common emitter amplifier in the next part of the experiment.

7.5 DESIGNING OF CE AMPLIFIER

In this part of the experiment you will design and build a transistor amplifier circuit using an $n-p-n$ transistor in universal bias arrangement. First we will recapitulate the universal biasing circuit of a transistor in common emitter configuration. Then you will determine the values of resistors and capacitors required to build the amplifier circuit. Here we will give an example to demonstrate, how to calculate the component values. However, you may have to modify the calculations depending the specifications of available transistor, power supply etc. in your laboratory.

7.5.1 Biasing the BJT Amplifier Circuit

You have learnt in Unit 4 of the theory course of Digital and Analog Circuits and Instrumentation (BPHE-143) about the biasing of transistor in common emitter configuration.

You have studied in Sec. 4.3 of Unit 4 of the theory course BPHET-143 that the selection of quiescent operating point is of vital importance to ensure that the transistor operates in the linear region of the typical output characteristics as shown in Fig. 7.7. Here we assume the emitter resistance R_E to be zero

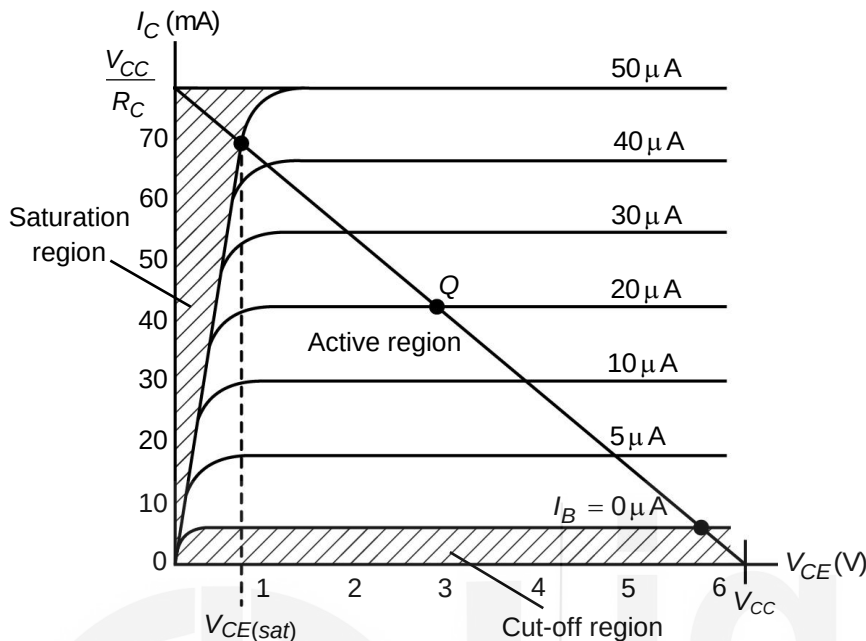


Fig. 7.7: Output characteristics of a BJT in common emitter configuration.

In fact, the quiescent operating point Q should be selected so that it lies at the centre of the dc load line i.e.

$$I_{CQ} = \frac{1}{2} \frac{V_{CC}}{R_C} \quad (7.5)$$

and $V_{CEQ} = V_{CC} / 2 \quad (7.6)$

This will ensure proper behaviour in both positive and negative half cycles of operation when the sinusoidal input signal v_i is superimposed. Yet another critically important point is that the operating point shifts with changes in temperatures under actual working conditions. Unless controlled, this affects the performance of the amplifier. Several circuit arrangements are designed to prevent a shift in the operating point. These are called **biasing circuits**. In Unit 4 you have learnt that the best bias circuit to provide stability in common emitter configuration is the Universal bias circuit shown in Fig. 7.8.

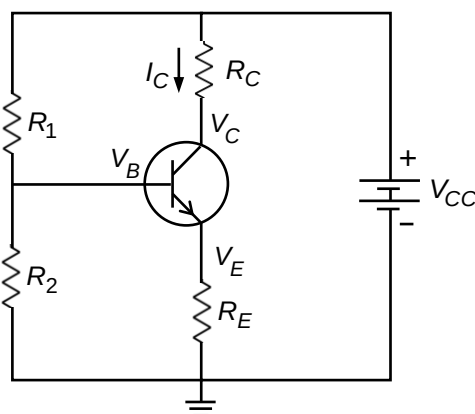


Fig. 7.8: Universal bias for an n - p - n transistor in CE configuration.

Here, to attain the stability of the Q point, we introduce a resistance R_E between the emitter and ground. The current in R_E causes a voltage drop which is in the direction to reduce the forward bias of the base-emitter junction. When I_C tends to increase (may be due to reasons like a rise in temperature), the current in R_E increases. This increases the voltage drop across R_E , which effectively reduces the forward bias of the base-emitter junction. As a result, the base current decreases. Hence, the collector current also decreases. Thus, the increase in I_C will get compensated.

This is the circuit you will be using to study the BJT as an amplifier. As an illustration we will now determine the values of the circuit elements for a typical amplifier operation.

7.5.2 Determining the Circuit Elements for a Universal Bias Arrangement

Now we design a class A amplifier in universal bias circuit. As you have learnt in Unit 4 of the theory course BPHE-143, the dc biasing determines the quiescent operating point Q of the amplifier circuit. We will assume the following values for illustration.

$$\beta_{dc} = 100$$

Here β_{dc} is the ratio of collector current to the base current ($\beta_{dc} = I_C / I_B$), i.e., it is the dc current gain.

Let us choose, supply voltage

$$V_{CC} = 12 \text{ V}$$

and, $R_C = 2 \text{ k}\Omega$, $R_E = 1 \text{ k}\Omega$

So that $R_C / R_E = 2$.

Now if we assume the quiescent collector-emitter voltage to be $V_{CC} / 2$, then the remaining $V_{CC} / 2$ drops across $(R_E + R_C)$. Hence,

$$I_{CQ} = \frac{1}{2} \frac{V_{CC}}{R_C + R_E} \quad (7.7)$$

$$\therefore I_{CQ} = \frac{12 \text{ V}}{2(1 \text{ k}\Omega + 2 \text{ k}\Omega)} = 2 \text{ mA}$$

and

$$I_{BQ} = I_{CQ} / \beta_{dc} = 2 \text{ mA} / 100 = 20 \mu\text{A} \quad (7.8)$$

$$\therefore I_{EQ} = I_{CQ} + I_{BQ} = 2.02 \text{ mA} \quad (7.9)$$

and

$$V_{EQ} = R_E I_{EQ} = 2.02 \text{ V} \quad (7.10)$$

Assuming $V_{BE} = 0.7 \text{ V}$ for a typical silicon transistor, the base voltage

$$V_{BQ} = V_{BE} + V_{EQ} = 0.7 \text{ V} + 2.02 \text{ V} = 2.72 \text{ V} \quad (7.11)$$

We indicate the quiescent values of voltage and current by a suffix Q . For example, V_{CEQ} , I_{CQ} etc.

And output voltage under no external input (ac) signal,

$$V_{CQ} = V_{CC} - R_C I_{CQ} = 12 \text{ V} - 4 \text{ V} = 8 \text{ V} \quad (7.12)$$

You must ensure that $V_{CQ} > V_{BQ}$ (in case of the $p-n-p$ BJT, $V_{CQ} < V_{BQ}$).

Further, considering the circuit containing R_1 and R_2 , we have

$$R_1(I + I_{BQ}) = V_{CC} - V_{BQ} \quad (7.13)$$

or

$$R_1(I + 20 \mu\text{A}) = (12 - 2.72) = 9.28 \text{ V}$$

and

$$IR_2 = V_{BQ} = 2.72 \text{ V}$$

$$\frac{R_1}{R_2} \cdot \frac{(I + 20 \mu\text{A})}{I} = \frac{9.28}{2.72}$$

If we consider $R_1 = nR_2$,

$$n(I + 20 \times 10^{-6} \text{ A}) = 3.4I$$

Obviously $n < 3.4$ for the above equation to be satisfied.

Let us select $n = 3$.

Then

$$(3.4 - 3.0)I = 0.4I = 3 \times 20 \times 10^{-6} \text{ A}$$

or

$$\begin{aligned} I &= (3 \times 20 \times 10^{-6} / 0.4) \text{ A} \\ &= 150 \mu\text{A} \end{aligned}$$

Hence,

$$R_2 = \frac{V_{BQ}}{I} = \frac{2.72 \text{ V}}{150 \times 10^{-6} \text{ A}} = 18.1 \text{ k}\Omega$$

and

$$R_1 = nR_2 = 3 \times 18.1 \text{ k}\Omega = 54.3 \text{ k}\Omega$$

In this way we have selected all the resistive elements. Now we have to connect

- i) a capacitor (C_C) at the collector to obtain the varying output voltage,
- ii) a capacitor (C_B) at the base to isolate V_{CC} from input ac signal source,
- iii) a capacitor (C_E) to shunt R_E so that E remains at ground.

All these capacitors should be high valued and for the present we can take high valued electrolytic capacitors. Thus, we take $C_E = C_B = C_C = 10 \mu\text{F}$.

With these selections, the exact circuit diagram becomes as shown in Fig. 7.9.

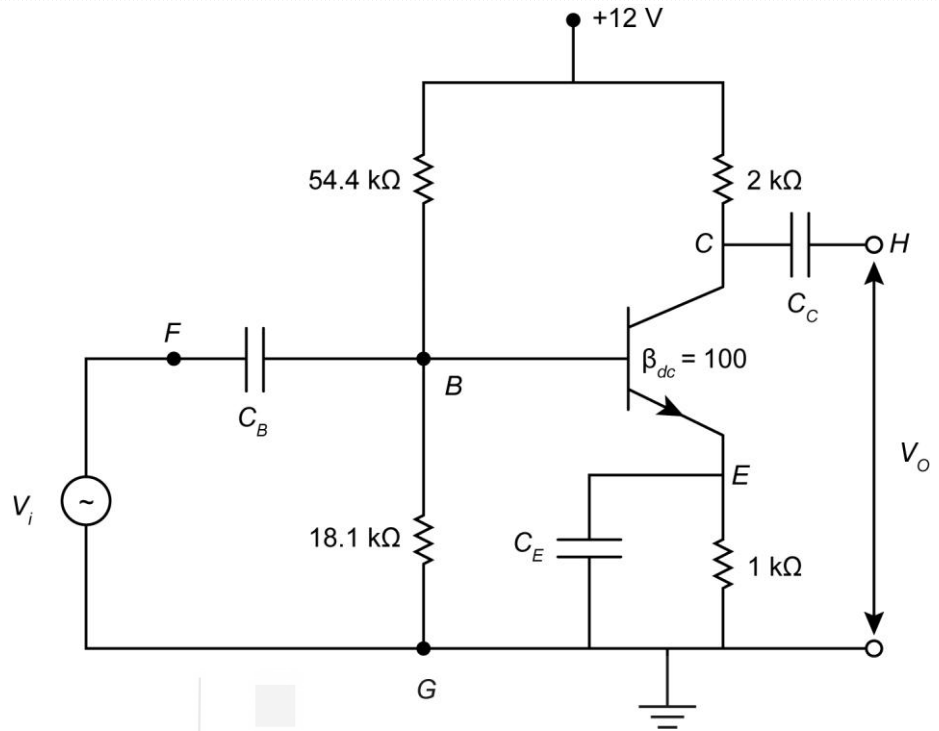


Fig. 7.9: Class A amplifier in a universal bias arrangement.

You should go through these calculations carefully so that you are able to generate other sets of element values, if required by the specifications of the apparatus available in your laboratory.

***SAQ 1* - Effects of β variation**

Suppose that β_{dc} of BJT being used has fallen to 75. Determine quiescent values of terminal currents/voltages. What effect will this change have on the performance of the amplifier?

7.5.3 Gain and Frequency Response of an Amplifier

After calculating the component values for your circuit, now you are ready to build the amplifier and test. However, before you start with the experiment, you must

- familiarise yourself with electronic instruments that you are going to handle, and
- recognise various circuit elements to be used.

Now, follow the procedure for setting up the circuit.

You can now study the BJT as an amplifier.

Procedure

Before you wire the circuit, answer the following questions:

- Have you identified the BJT?
- Have you calculated the elements values that you are using?

3. Have you understood the working of electronic instruments that you are using?

Proceed ahead only if answers to all these questions are in the affirmative. If not, consult the counsellor to get your doubts cleared.

1. Select the component values according to values of V_{CC} and β_{dc} prescribed, by following the procedure outlined in Sec. 7.5.2. The values of V_{CC} , I_C and β_{dc} will be determined by the BJT ratings and its static characteristic curves. This information will be available in your laboratory. Consult with your Counsellor in the laboratory for it. You may not get the exact values of the resistors desired. Select the values that fit closest to the desired ones.
2. Now connect the circuit as shown in Fig. 7.9 on a breadboard or by soldering on a printed circuit board (PCB) which will be available in the laboratory.
3. Measure V_{CEQ} , V_{EQ} and V_{BQ} by multimeter to check that measured values match the values calculated earlier. Proceed ahead only if such a match is obtained.
4. Now take an ac signal generator and adjust it so that it generates sinusoidal voltage. Keep its output voltage level in the mV range and frequency in the range of 1 kHz.

We suggest that you should use the CRO to measure various ac voltages using its AC mode. It will be better if you could check the output waveform of the signal generator and measure its amplitude by CRO at this stage itself.

5. Now connect the high and low output terminals of the signal generator to F and G points shown in Fig. 7.9, respectively.
6. Connect the Y input terminals of CRO also to these points (for convenience, connect the ground terminal to G while keeping its high terminal probe free. The required connection may now be made by touching F with the High Terminal Probe (HTP) of CRO. Select the voltage range of mV on the CRO control panel. Adjust the time base of CRO to get a steady waveform.
7. Adjust output amplitude selector knob of the signal generator till you get a steady signal with value 10 mV. This is the input voltage (v_i).
8. Remove HTP from F and move the voltage range selector knob of CRO to volt range.
9. Now touch the CRO probe to point H at the output of the amplifier circuit. If your connections are right you will observe a sinusoidal wave with steady voltage. (Reduce the level of input signal if you get a distorted waveform). In such a case repeat measurement of v_i done at Step No. 7. Measure this output voltage (v_o).
10. With values of input and output voltages measured as described above, calculate the voltage amplification factor of the amplifier from the ratio

$$A = v_o / v_i$$

This gives you the value of the voltage gain at a frequency 1 kHz. You should move ahead only if A is sufficiently high. Otherwise, check the circuit connections till you get a satisfactory result. If the trouble persists, consult with your Counsellor.

SAQ 2 - Testing of CE amplifier

- Keep the frequency of the input signal at 1 kHz. Measure output voltage and leave the CRO connection in this state. Now take a resistor of value equal to R_E and connect it in parallel with R_E . (You can just touch the ends of R_E with the ends of this new resistor). Observe the change in v_o and try to explain the reasons.
- Repeat part (a) but now connect resistors of values say 0.5 k Ω , 1 k Ω , 5 k Ω in succession across GH in Fig. 7.9.
- Keep the frequency of the input signal at 1 kHz and adjust CRO to measure the output voltage v_o . Now increase the voltage level of input signal and observe output waveform. Do you observe any distortion in the output signal? What is your inference out of these observations?

- Adjust the output signal frequency selector knob of signal generator to 100 Hz and repeat the steps 6 to 10.
- Carry out such measurements to scan a wide frequency band from 100 Hz to 100 kHz as suggested below at suitable frequency intervals.

Frequency Range	Interval
100 Hz – 1 kHz	100 Hz
1 kHz – 20 kHz	1 kHz
20 kHz – 100 kHz	10 kHz

Record these observations in an Observation Table 7.5. Thus, you have obtained the gain of the amplifier over a wide frequency range. You should now record observations as suggested below.

Observations

Identifying number of BJT :

Type of BJT :

β_{dc} of BJT =

V_{CC} applied = ... V

Calculated values of

$R_1 = \dots$; $R_2 = \dots$; $R_C = \dots$; $R_E = \dots$

Calculated values of

$I_{BQ} = \dots$; $I_{CQ} = \dots$; $V_{CEQ} = \dots$; $V_{EQ} = \dots$

$V_{BQ} = \dots$; $V_{CQ} = \dots$

Experiment 7 Study of Transistor Characteristics in CE Mode and Design of CE Amplifier

Actual values of circuit elements used

$$R_1 = \dots ; R_2 = \dots ; R_C = \dots ; R_E = \dots$$

$$C_C = \dots ; C_B = \dots ; C_E = \dots$$

Measured values of

$$V_{CEQ} = \dots ; V_{EQ} = \dots ; V_{BQ} = \dots ; V_{CQ} = \dots$$

Observation Table 7.5: Study of variation of voltage amplification factor with frequency

No. of observation	Frequency of the signal	Input voltage v_i (in mV)	Output voltage v_o (in mV)	Voltage gain $A = v_o / v_i$
1.				
2.				
3.				
4.				
5.				
6.				

Draw a graph on semi-log graph paper with frequency on the logarithmic x-axis and gain A on y-axis. The curve obtained by you is called the **frequency response curve** of the amplifier.

Report your results by answering the following questions:

- Does this curve remain flat over the entire frequency range?
- If not, what is the change?
- Which is the frequency region in which the change is more apparent?
- Taking the gain at mid frequency region (say 5 kHz) as the mean (A_m).

Find the frequencies at which the gain has fallen to $\frac{A_m}{\sqrt{2}}$? Hence calculate the bandwidth.

APPENDIX 7A: SOME COMMON TRANSISTOR PACKAGES

Fig. 7A.1 shows typical configurations of E , B and C in the transistor in side and bottom views. This would help you to identify different kinds of transistors.

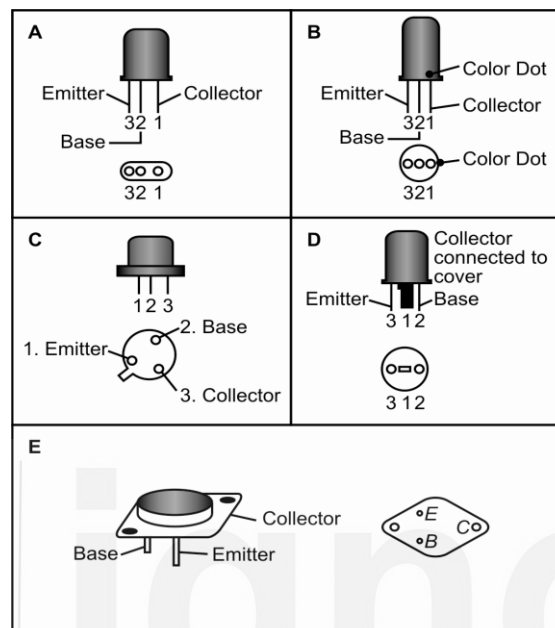


Fig. 7A.1: Identifying some common transistor packages.

EXPERIMENT 8

DESIGN OF OP AMP INVERTING AND NON-INVERTING AMPLIFIERS

Structure

- | | | | |
|-----|-----------------------------|-----|-------------------------|
| 8.1 | Introduction | 8.4 | Inverting Amplifier |
| | Expected Skills | 8.5 | Non-Inverting Amplifier |
| 8.2 | Basics of Op Amp | | |
| 8.3 | Negative Feedback in Op Amp | | |

8.1 INTRODUCTION

Given below is a list of some systems and equipment that you must have seen and / or used in your everyday life.

- a) A radio set
- b) A public address system
- c) An electrocardiography (ECG) machine
- d) A microscope

Do you find something common in all the above equipment? The answer is “*some sort of an amplifier*”. In a radio set, we have an amplifier which amplifies very small electrical signals (of the order of a few millivolts). These signals are received from distant radio stations. Not only that, you can even change the amplification by turning the volume control. In a public address system, speech is given to the microphone by the person speaking. Speech is converted into electrical signals, amplified and fed to the loudspeaker. In an ECG, we have amplification of small electrical signals (a few microvolt) given out by the heart. A microscope

is an optical instrument to see amplified (magnified) images of very small, microscopic objects. Thus, in all above examples, we have some type of **amplifier**.

In this experiment you will use a special type of amplifier, to amplify electrical signals, called an **Operational Amplifier** (OP AMP). You have studied about the op amp and its applications in Unit 13 and 14 of the theory course BPHEL-143. You know that an op amp may be treated as a multipurpose device which can be used as amplifier, oscillator, differentiator, integrator, and can also perform other mathematical operations like addition, subtraction, multiplication etc. (and hence the name op amp). They are very extensively used in present day electronics ranging from entertainment electronics to medical instrumentation and computers.

You will carry out some simple experiments using op amp illustrating some of its elementary characteristics.

Expected Skills

After performing this experiment, you will be able to:

- ❖ build and test an inverting amplifier of desired gain using op amp; and
- ❖ design and build a non-inverting amplifier of desired gain and test the circuit.

For this experiment, you will require following apparatus and components.

Apparatus Required

Variable power supply of ± 15 V, dry cell of 1.5 V, voltmeter for dc measurement – 2 no., rheostats or potentiometer of 10 k Ω , resistors (10 k Ω , 50 k Ω), half-watt resistor of different values (like 4.7 k Ω , 10 k Ω) – 1 no. each, an op amp IC 741C, breadboard and connecting wires.

8.2 BASICS OF OP AMP

Most commonly used op amp in integrated circuit (IC) form is IC 741C. The symbol used for op amp is shown in Fig. 8.1. It is a triangle pointing to the signal flow. This symbol also shows the terminal (or pin) numbers for a general purpose and very popular op amp integrated circuit – IC 741C. All op amps have at least five terminals – two for inputs, two for power supply and one for the output. General purpose 741C has some other terminals as well.

The op amp has two input terminals. Pin 2 is the inverting input. When the input is given to it, the output at pin 6 is available with 180 degree phase change. Pin 3 is the non-inverting input. The input given to this pin is available at pin 6 without phase change. The inverting input (pin 2) is often shown with a (–) sign and non-inverting input (pin 3) with a (+) sign. These two terminals are known as **differential input terminals**. The output voltage depends upon the difference in voltages between them.

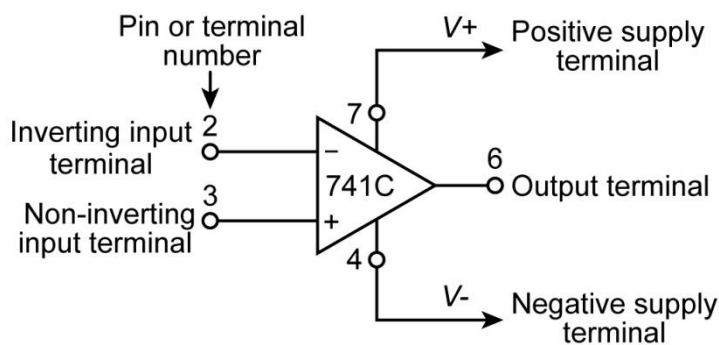


Fig. 8.1: Symbol for an op amp.

The op amp requires a dual power supply; means a positive as well as negative voltage supplies are used. Negative voltage terminal of the dual power supply is connected to pin 4 and positive voltage terminal is connected to pin 7. Note that if the polarities of the voltages applied to pins 4 and 7 are reversed, the op amp shall be damaged and cannot be used any more.

SAQ 1 – Pins of op amp

What are the numbers of input and output pins of IC 741C?

The op amp IC is housed in a suitable package. Op amp 741C is available in two most popular packages (a) metal can and (b) dual in-line packages (DIP). These packages are shown in Fig. 8.2a and b respectively. This IC has eight pins (or terminals) to connect it in the circuit. The metal can IC is round in shape and pin number 8 is indicated by a tab protruding out from the metal package. The DIP packages are in plastic casing. Pin number 1 is indicated by circle or dot engraved on the top of the IC package.

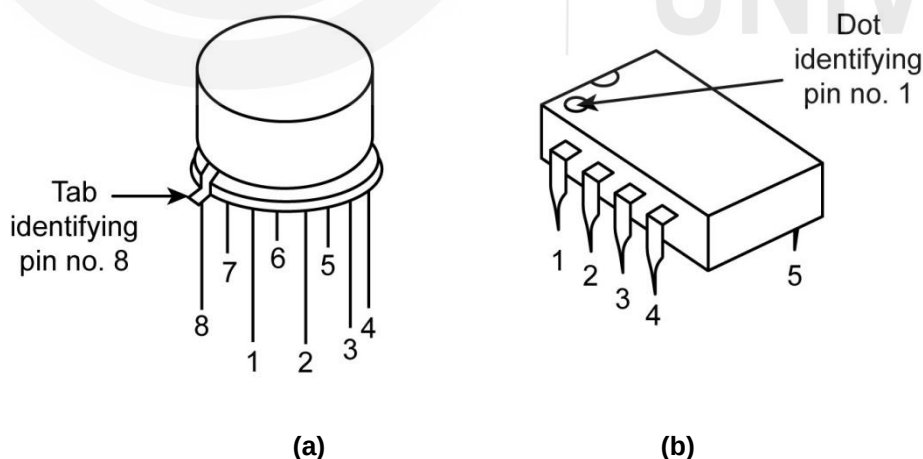


Fig. 8.2: Op amp packages: a) metal can; b) 8-pin DIP package.

The pin count of every IC including op amps is done as follows. Look at the top view of the IC and note the position of a notch or a dot in case of DIP and a tab in case of a metal can package. The first pin on the left hand side of the notch or dot or tab identifies the pin 1. Then other pins are counted counter-clockwise. If you see the IC in its bottom view, then this counting scheme is

reversed. That is in bottom view, the next pin on the right side of the tab or dot is Pin 1 and the counting is done from 1 to 8 in clockwise direction.

Precautions while Handling Op Amp IC

You will build the circuit in which op amp is being used either on a breadboard or on a printed circuit board. There are certain precautions to be taken while constructing and using the circuit.

- While doing the entire wiring of the circuit keep the power supply off.
- Use wires of appropriate length. Avoid using too long wires.
- All ground connections should meet at a common electrical point.
- While starting the circuit, first of all, power ($\pm V$) should be supplied to the op amp.
- Apply signal to the input pins only after op amp is supplied with power.
- Always measure voltages and not currents. The current may be calculated by finding voltage at two ends of a resistor.
- When the work is over, remove signal first and then switch off the op amp power supply.

It is necessary here to stress further that **never**

- reverse the polarity of supply voltages given to IC pins;
- apply input signal voltages greater than $+V$ and less than $-V$,
- connect any signal to input pins with op amp power supply off.

You have learnt about the characteristics of op amp in Unit 13 of the theory course. Now we will briefly discuss about the feedback used in op amp circuits.

8.3 NEGATIVE FEEDBACK IN OP AMP

While using the op amp as a comparator, we used its property of infinite open loop gain. However, if we can control the gain of the op amp, then many more other applications of op amp can be implemented.

You know that negative feedback reduces the gain of an amplifier. Negative feedback can be obtained if the signal fed back from the output is in opposite phase of the input signal. In op amp, you know that the inverting input is in opposite phase of the output. Hence, if we feed a part of the output signal to this input through a feedback network, we can achieve the negative feedback configuration of an op amp circuit. Fig. 8.3a and b show the two possible configurations of op amp negative feedback circuits.

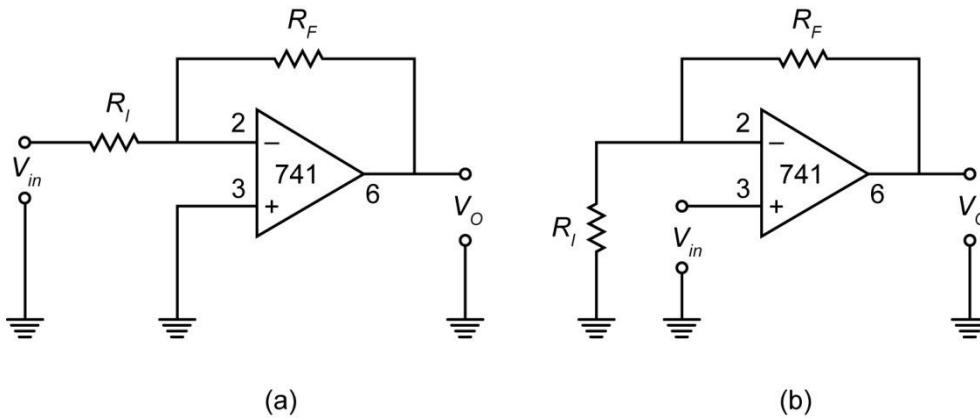


Fig. 8.3: Negative feedback circuits of op amp with input given to a) inverting input; b) non-inverting input.

In both these circuits, the feedback is given to the inverting input through a feedback resistor R_F . In certain applications, this resistor may be replaced by another device like capacitor, as you will do while performing the next experiment on integrator circuit.

With this background about the op amp circuits with negative feedback, now we will turn to the experiment, which you will perform in two parts. In the first part of the experiment you will design, build and test an inverting amplifier and in the second part of the experiment, you will work with a non-inverting amplifier.

8.4 INVERTING AMPLIFIER

Consider the circuit shown in the Fig. 8.4. In this circuit the output pin 6 is connected through a resistor R_F to the inverting input pin 2. The input voltage is given to pin 2 through an input resistor R_I . The non-inverting input pin 3 is grounded. This is similar to the circuit shown in Fig. 8.3a. The output pin 6 is also grounded through the load resistor R_L .

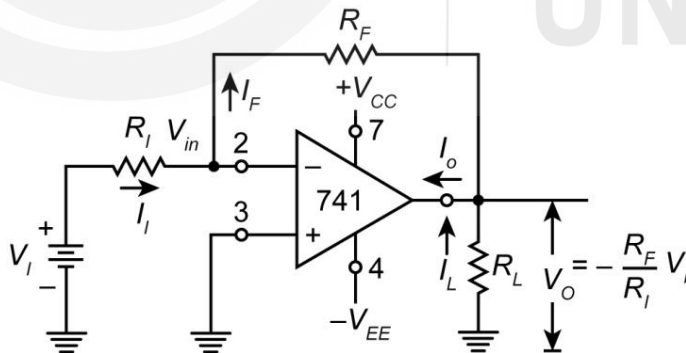


Fig. 8.4: Inverting amplifier.

While analysing this circuit, we make the following two important assumptions based on the properties of ideal op amp:

- Due to infinitely large gain of the op amp, the finite output (lesser than V_{SAT}), is obtained only if the difference between the inputs (V_D) is zero.
- The input impedance of op amp is infinite, hence no current flows into the input terminals of the op amp.

Although, these assumptions are based on the ideal op amp characteristics, even for practical op amps these are applicable quite satisfactorily.

A positive input voltage ($+V_I$) is applied to the inverting ($-$) input pin 2 through input resistor R_I and the feedback resistor R_F provides the necessary feedback from the output to the input. The non-inverting input is at ground potential (0 V). As per the first assumption, because non-inverting (+) input (pin 3) is grounded, pin 2 is also at ground voltage (0 V). Thus though pin 2 is not connected to the ground, yet it appears to be grounded. Therefore, the inverting input is said to be at **virtual ground**. You must remember that because of virtual ground, under negative feedback, the inverting terminal always remains at the same voltage, as that at the non-inverting terminal. This is very important concept and will come handy to analyse all negative feedback op amp circuits.

In the circuit of Fig. 8.4, the current through R_I is decided by the voltage drop across it. One end of R_I is connected to $+V_I$ and another end is at 0 V due to virtual ground concept. Therefore, the voltage drop across R_I is $+V_I$. The input current, I_I , flowing through R_I from a point of higher potential to a point of lower potential (i.e. pin 2 which is at 0 V) is

$$I_I = \frac{V_I}{R_I} \quad (8.1)$$

Now, as per our second assumption, no current can enter the op amp. Therefore I_I has to flow through R_F . Therefore, I_F , the current flowing through R_F is equal to I_I . That is $I = I_I = I_F$. Thus the voltage drop across R_F is

$$V_F = IR_F \quad (8.2)$$

Putting for I from Eq. (8.1) we get

$$V_F = \frac{V_I}{R_I} R_F \quad (8.3)$$

Since pin 2 is at virtual ground, R_L is in parallel with R_F . Therefore, the magnitude of V_F is equal to V_O . But V_F is negative because the current flows from pin 2 (which is at 0 V) to pin 6. Thus, V_O the voltage between pin 6 and ground is

$$\begin{aligned} V_O &= -V_F \\ &= -\frac{V_I}{R_I} R_F = -\frac{R_F}{R_I} V_I \quad (\text{using Eq. 8.3}) \end{aligned}$$

The closed loop gain of the amplifier, A_{CL} , is

$$A_{CL} = \frac{V_O}{V_I} = -\frac{R_F}{R_I} \quad (8.4)$$

Thus A_{CL} depends on R_F and R_I only and does not depend on the open loop gain of the operational amplifier. Since A_{CL} is negative, this configuration of the amplifier is called **inverting amplifier**. The choice of R_F and R_I is in

the hands of the designer and the gain of practically any value can be obtained. In all practical applications the value of R_I should be chosen to be large, say $10\text{ k}\Omega$, so that it does not short out the input resistance of the op amp.

You must have realised that the inverting amplifier circuit can be used for multiplication and division. The output voltage is R_F / R_I times the input voltage. If the input voltage represents some number then the output voltage will be equal to that number multiplied by the factor R_F / R_I . The ratio R_F / R_I is under our control and can assume any value. With $R_F > R_I$ we can use the inverting amplifier for multiplication. By making R_I greater than R_F it can be used for division.

Now follow the given steps to build the inverting amplifier using IC 741C.

You have to build an inverting amplifier using op amp with a nominal gain of -5 . You can use the circuit shown in Fig. 8.5. Choose $R_I = 10\text{ k}\Omega$.

From Eq. (8.4),

$$R_F = A_{CL} \times R_I$$

with $A_{CL} = (-)5$

$$R_F = 5 \times 10\text{ k}\Omega = 50\text{ k}\Omega$$

You can choose $R_L = 10\text{ k}\Omega$ for limiting the output current of the op amp IC.

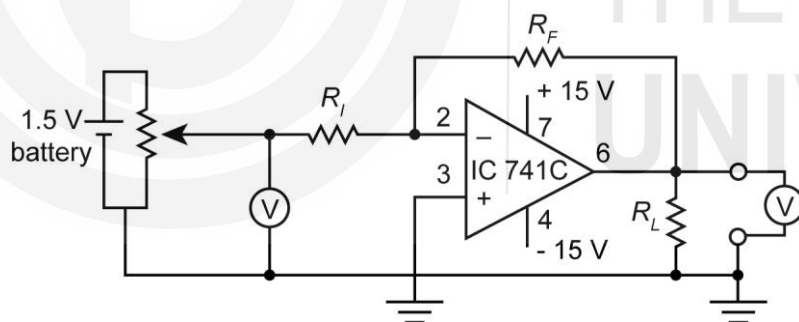


Fig. 8.5: Inverting amplifier.

1. Place the IC on the breadboard.
2. Connect $R_I = 10\text{ k}\Omega$, $R_F = 10\text{ k}\Omega$, $R_L = 10\text{ k}\Omega$
3. Connect $+15\text{ V}$ supply to pin 7 and -15 V to pin 4.
4. Adjust rheostat connected to 1.5 V cell so that voltage reading in the input voltmeter is zero.
5. Switch on the power supply and measure the voltage at the output and note it. It may be treated as zero error.
6. By varying the rheostat, change the input voltage. This will also change the output voltage. Take readings of input V_I and output V_O voltages for different settings of rheostat and note them in the Observation Table 8.1.

7. Reduce the input voltage to zero and switch off the power supply.
8. Reverse the polarity of battery cell (1.5 V) and repeat the steps 4 to 7 for reversed polarity of input voltage.

Observation Table 8.1: Op amp inverting configuration

$$50\text{ k}\Omega\ R_I = 10\text{ k}\Omega, R_F = 50\text{ k}\Omega$$

Input V_I (V) with polarity	Output V_O (V) with polarity	Gain $= \frac{V_O}{V_I}$ with polarity	Phase
+0.25			180°
+0.50			"
+0.75			"
+1.00			"
+1.25			"
+1.50			"
-0.25			"
-0.50			"
-0.75			"
-1.00			"
-1.25			"
-1.50			"

Mean Gain = ...

Result: Gain of the inverting amplifier:

Calculated = ...

Observed = ...

SAQ 2 – Error in the inverting gain

Are the observed and calculated gains matching? If not, what could be the reason? 741C?

8.5 NON-INVERTING AMPLIFIER

The circuit given in Fig. 8.6 is for a non-inverting amplifier. You must have noticed that it is similar to the circuit shown in Fig. 8.3b. In this circuit R_I continues to be connected as in the case of inverting amplifier except that it is connected to ground and the input voltage V_I is given to the non-inverting (+) input at pin 3.

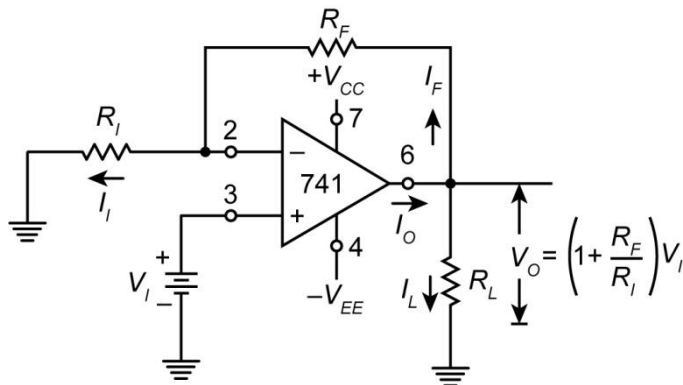


Fig. 8.6: Non-inverting amplifier.

As discussed in the last section, due to virtual ground, the inverting input pin 2 is also at the same voltage at which non-inverting input pin 3 is. Thus, pin 2 is at V_I which sets the current I_I through R_I . The voltage drop across R_I , being V_I , we get

$$I_I = \frac{V_I}{R_I} \quad (8.5)$$

Obviously, I_I flows from pin 2 to the ground. Since no current flows in the op amp, I_F the current flowing through R_F has to be equal to I_I , i.e.

$I = I_I = I_F$. Thus, the current I flows from output terminal pin 6 to pin 2 to ground. Hence, the output pin 6 is at a greater potential than pin 2. Since the load resistor R_L is now in parallel with the series combination of R_I and R_F therefore the output voltage is equal to the sum of voltage across R_I and R_F . Thus

$$\begin{aligned} V_O &= V_I + IR_F \\ &= V_I + \frac{V_I}{R_I} R_F \quad (\text{using Eq. 8.5}) \end{aligned}$$

Or the closed loop gain of the amplifier is

$$A_{CL} = \frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_I}\right) \quad (8.6)$$

You must have noticed that A_{CL} has the same sign as the input voltage V_I i.e. positive. For this reason, we call this amplifier a **non-inverting amplifier**. In this case also the gain depends upon the values of R_F and R_I and not on the parameters of the operational amplifier. Remember that here the gain is always greater than unity. The ratio R_F / R_I can be made as small as possible and the gain can be made close to unity, but it can never be less than unity. Pin 6 being at a potential greater than the ground potential, the load current I_L flows from pin 6 to ground through the load resistor R_L .

Procedure

You have to design a non-inverting amplifier using op amp IC 741C for gain of + 10. Choose $R_I = 10 \text{ k}\Omega$.

From Eq. (8.6), you can calculate

$$R_F = 1 + (A_{CL} - 1)R_I$$

$$= (10 - 1) \times 10 \text{ k}\Omega = 90 \text{ k}\Omega$$

Choose $R_L = 10 \text{ k}\Omega$.

Connect the circuit as shown in Fig. 8.7.

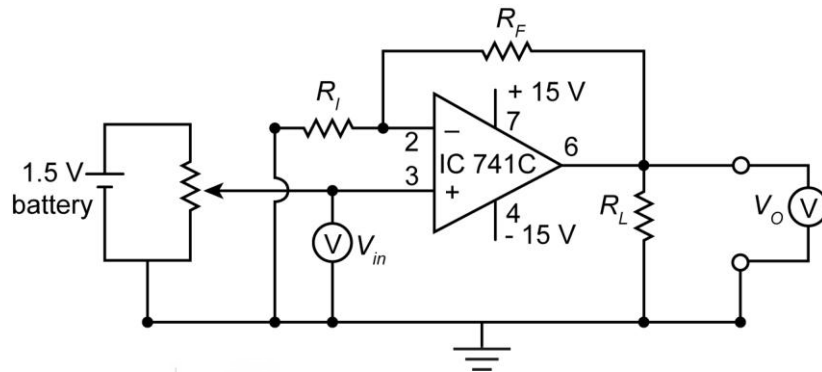


Fig. 8.7: Non-inverting amplifier.

You have to follow similar steps to perform this part of the experiment, as done in case of inverting amplifier.

You should prepare Observation Table 8.2 similar to Observation Table 8.1 and record the output voltage for different input voltages (of both polarities obtained by reversing the battery connections). Calculate the mean gain from the observed gain values.

Calculate the expected gain from the circuit by measuring the values actually used resistors and substituting them in Eq. (8.6).

Result: Calculated gain = ...

Observed gain = ...

SAQ 3 – Error in the non-inverting gain

Comment on the difference in the calculated and observed values of the gain of a non-inverting amplifier.

EXPERIMENT 9

DESIGN OF OP AMP DIFFERENTIATOR AND INTEGRATOR

Structure

9.1	Introduction Expected Skills	9.3	Differentiator using Op Amp IC 741C
9.2	Integrator using Op Amp IC 741C	9.4	Conclusion

9.1 INTRODUCTION

You must have used electronic calculators, or computers at some stage. How does a computer perform mathematical operations? In fact some electronic circuits are designed to perform the various mathematical calculations. Examples of such circuits are integrators and differentiators. In these circuits, if you apply any electrical signal at the input, you will get its integrated or differentiated form at the output. These circuits are extremely useful in computing, signal processing and signal generating applications. Operational amplifiers can be used for such applications.

In this experiment you will build and test integrators and differentiators using IC 741C.

Expected Skills

After performing the experiment, you will be able to:

- ❖ build a circuit to integrate a signal using an op amp;
- ❖ display the integrated signals of sine and square wave inputs on CRO;
- ❖ build a circuit to differentiate a signal using an op amp;
- ❖ display the differentiated sine and square wave signals on CRO; and
- ❖ compare the expected and observed integrated and differentiated signals.

You will require the following components and apparatus to perform this experiment.

Apparatus Required

IC 741C, dual power supply (± 15 V), several values of resistor and capacitors, signal generator giving sine and square waves of various frequencies, dual trace oscilloscope (CRO), breadboard, connecting wires.

You will perform this experiment in two parts. In the first part you will design and build an integrator and in the second part a differentiator.

9.2 INTEGRATOR USING OP AMP IC 741C

You have studied about the integrator using op amp in Unit 14 of theory course BPHE-143.

Fig. 9.1 shows the circuit of a basic integrator which performs the mathematical operation of integration. The output waveform, V_O , is the integral of the input waveform, V_I .

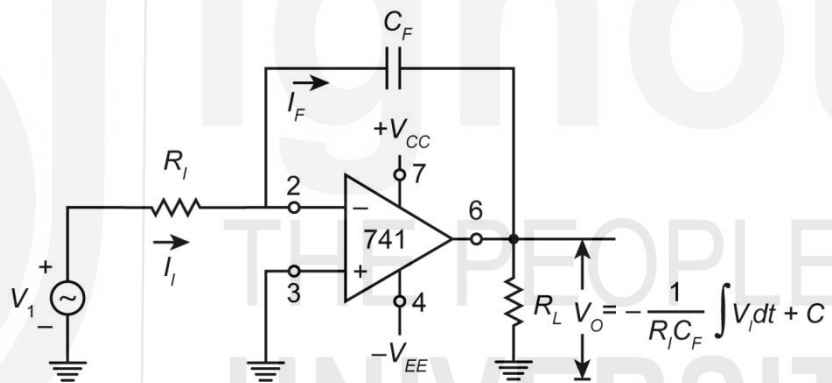


Fig. 9.1: Basic integrator.

The integrator circuit is obtained by replacing the resistor R_F by a capacitor C_F in the circuit of inverting amplifier, while rest of the circuit remains the same. Based on the basic assumptions made for negative feedback op amp circuits, the current I_I flowing through the resistor R_I has to be equal to the current I_F flowing through the capacitor C_F . Thus

$$I_I = I_F$$

Current I_I flows from the input signal generator to pin 2 and from there it flows through the capacitor C_F . Pin 2 being at 0V, the voltage drop across R_I is V_I and that across C_F is $-V_O$. Therefore,

$$I_I = \frac{V_I}{R_I}$$

and
$$I_F = C_F \frac{d(-V_O)}{dt}$$

Hence we can write,

$$\frac{V_I}{R_I} = C_F \frac{d(-V_O)}{dt}$$

or

$$V_I = -R_I C_F \frac{d(-V_O)}{dt}$$

On integrating this equation, we get

$$\int V_I dt = -R_I C_F V_O$$

$$\therefore V_O = -\frac{1}{R_I C_F} \int V_I dt \quad (9.1)$$

Eq. (9.1) shows that the output is directly proportional to the integral of the input voltage waveform. If the product $R_I C_F$ is made equal to 1, then we get

$$V_O = -\int V_I dt \quad (9.2)$$

In practical integrator circuit, a large value resistor R_F is connected in parallel with C_F to provide a parallel feedback path and avoid the charging of capacitor to V_{SAT} value.

In this experiment you will design an integrator with gain 10 (you may choose other gain value depending on the available components in discussion with your Counsellor.)

So, if you choose $C = 1 \mu F$, then, $R = 100 k\Omega$, you should add a resistor of about $220 k\Omega$ parallel to the capacitor. The circuit after connecting the calculated components will look like the one shown in Fig. 9.2.

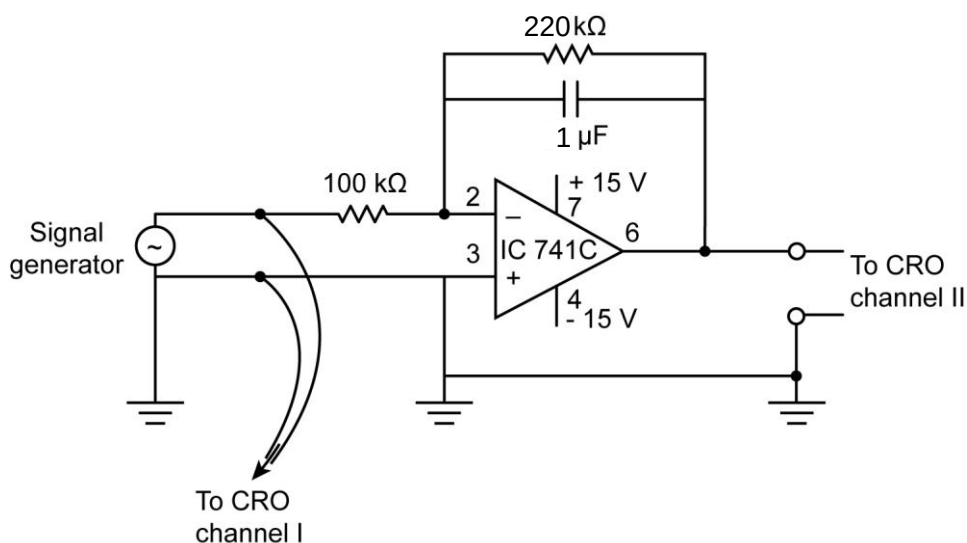


Fig. 9.2: Op amp integrator circuit using IC 741C.

Perform the following steps to build and test the integrator.

Procedure

1. Assemble the circuit on a breadboard and connect ± 15 V supply properly.
2. Connect the signal generator output to the channel I input of oscilloscope. Select sine wave output and adjust the amplitude to 0.5 V and frequency to 1 kHz.
3. Connect the signal generator output to the input of the op amp circuit.
4. Connect the Channel II of the oscilloscope to the output of the circuit.
5. Synchronise the input and output signals on the screen of the oscilloscope by adjusting vertical positions of both the traces.
6. Measure the input and output signal amplitude and frequency. Trace the input and output waveforms on the CRO screen using a tracing paper. Also note the V/div and time base settings of the CRO on this paper.
7. Change the frequency and amplitude of the input signal and again measure the output voltage and frequency repeating steps (2) to (5). Record your readings in Observation Table 9.1.
8. Repeat the experiment using square wave input from the signal generator and record your observations in the Observation Table 9.2.
9. Take the traces of input and output on CRO displays for square waveforms also.

Observation Table 9.1: Integration of sine wave

S.No.	Input Amplitude (V)	Input Frequency (Hz)	Output Amplitude (V)	Output Frequency (Hz)
1.				
2.				
3.				
4.				
5.				

Observation Table 9.2: Integration of square wave

S.No.	Input Amplitude (V)	Input Frequency (Hz)	Output Amplitude (V)	Output Frequency (Hz)
1.				
2.				
3.				
4.				
5.				

If the input waveform is a sine wave then the output waveform should be a negative of inverted cosine wave, which means that it is a normal cosine wave as shown in Fig. 9.3a. If the input waveform is a square wave, then the output waveform should be a triangular wave as shown in Fig. 9.3b.

You know that for a sine wave

$$\int \sin x \, dx = -\cos x$$

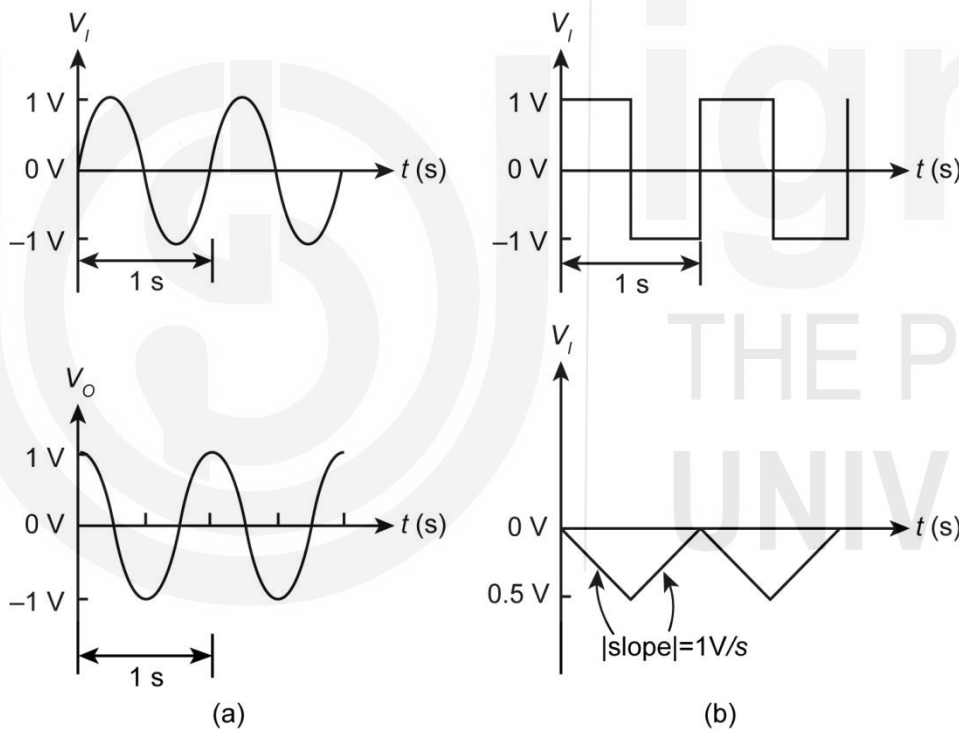


Fig. 9.3: Output of a basic integrator when input is a) sine wave; b) square wave.

Confirm that the traced waveforms from CRO display are matching with the above waveforms. If there is a difference from the expected waveforms, find out and write down the reasons.

After testing the integrator circuit, now you should build and test differentiator circuit in the next part of the experiment.

9.3 DIFFERENTIATOR USING OP AMP IC 741C

Fig. 9.4 shows the circuit for basic differentiator which performs the mathematical operation of differentiation. The output waveform is the derivative of the input waveform.

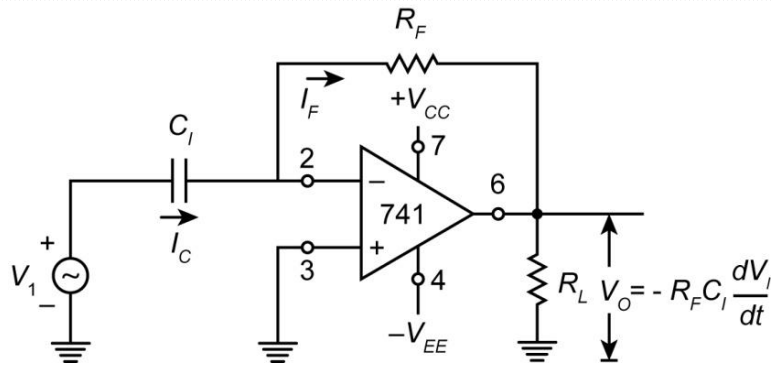


Fig. 9.4: Basic differentiator.

The differentiator circuit is obtained by replacing R_I of an inverting amplifier by a capacitor, while rest of the circuit remains the same. Just like in the case of inverting amplifier, the current I_C flowing through the capacitor C_I should be equal to the current I_F flowing through the resistor R_F . Thus

$$I_C = I_F$$

The current I_C flows from the input signal source (V_I) to pin 2 from where it flows through R_F . Pin 2 being at 0 V due to virtual ground, the voltage drop across C_I is V_I and the drop across R_F is $-V_O$.

You can recall that the current flowing through a capacitor C is C times the rate of change of voltage across the capacitor. Therefore

$$I_C = C_I \frac{dV_I}{dt}$$

and

$$I_F = -\frac{V_O}{R_F}$$

Since

$$I_C = I_F,$$

$$C_I \frac{dV_I}{dt} = -\frac{V_O}{R_F}$$

Rearranging the terms, we get

$$V_O = -R_F C_I \frac{dV_I}{dt}$$

If the product $R_F C_I = 1$, then

$$V_O = -\frac{dV_I}{dt} \quad (9.2)$$

Thus the output voltage is the negative derivative of the input voltage V_I .

You should build a differentiator for typical gain depending on the component availability, under the instructions of your counsellor.

For gain = 2, if you choose $C_I = 1\mu\text{F}$, then $R_F = 2\text{M}\Omega$.

Build the circuit of a differentiator (Fig. 9.4) with IC 741C and components of desired values as done in the last part of the experiment.

Record your readings in Observation Table 9.3 for sine wave input and in Observation Table 9.4 for square wave input.

Trace the input and output waveforms in both the cases on the tracing paper noting the time base and V/div settings of CRO.

Observation Table 9.3: Sine wave input to a differentiator

S.No.	Input Amplitude (V)	Input Frequency (Hz)	Output Amplitude (V)	Output Frequency (Hz)
1.				
2.				
3.				
4.				
5.				

Observation Table 9.4: Square wave input to a differentiator

S.No.	Input Amplitude (V)	Input Frequency (Hz)	Output Amplitude (V)	Output Frequency (Hz)
1.				
2.				
3.				
4.				
5.				

If the input is a sine wave, then the output waveform will be a negative of cosine wave; and if the input is a square wave, then the output will be a spike waveform; with 180° phase shift, as shown in the Fig. 9.5.

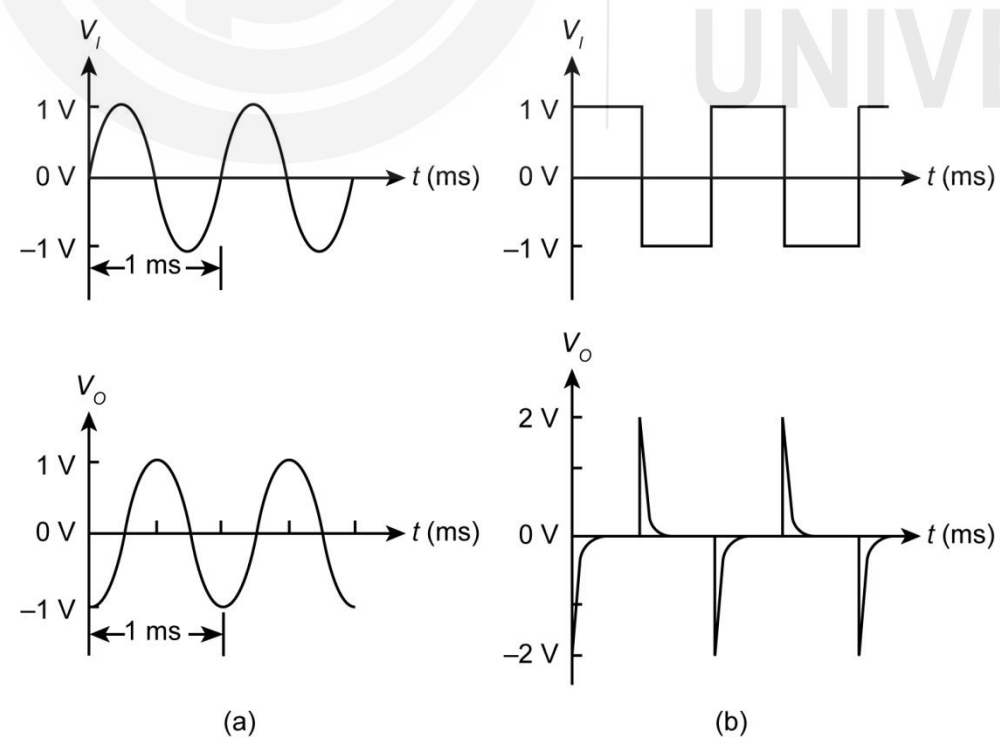


Fig. 9.5: Output of a basic differentiator when input is a) sine wave; b) square wave.

Results:

Compare the scans traced on the tracing paper with the expected scans of differentiated sine and square waves.

Are they matching?

If not state the reasons for the deviation of observed signals from the expected results.

9.4 CONCLUSIONS

You have learnt the way to integrate and differentiate sinusoidal and square waveforms. Now, write your conclusions in the form of answers to the following questions based on your observations.

- a) What happens to the fast-rising portions of the waveform after integration?
- b) What response do you get when you apply a dc voltage to the input of the differentiator?
- c) Which circuit smoothes the waveform?
- d) Which circuit picks up sharp variations in the input?

EXPERIMENT 10

DESIGNING AND BUILDING A PHASE SHIFT OSCILLATOR

Structure

- | | | | |
|------|--|------|--|
| 10.1 | Introduction
Expected Skills | 10.3 | Building and Testing a Phase Shift
Oscillator |
| 10.2 | Phase Shift Oscillator Fundamentals
Phase Shift
Phase Shift Oscillator Circuit | | |

10.1 INTRODUCTION

You have learnt in Unit 11 of theory course on Digital and Analog Circuits and Instrumentation (BPHE-143) that an oscillator is a circuit that converts dc form of electric power into ac. The output waveform of an oscillator is essentially periodic in nature. Frequently oscillators produce sine waveform or square waveforms. Sine wave oscillators are harmonic in the sense that their output waveform is similar to the displacement-time curve of a particle performing SHM (Simple Harmonic Motion); and have a unique frequency. While sine waveforms have dominated the world of analog electronics for a long time, the square waveform is predominant in today's world of digital electronics, electronic communication and computers. Since a square wave itself contains a mixture of multiple frequencies, oscillators producing square wave output do not qualify for the term harmonic oscillators.

Oscillators are used in transmitters, receivers, quartz watches and clocks, metal detectors, computer systems and in industrial process control / automation too. There is a vast range of frequencies needed to be produced in such applications ranging from once in a day to billions of cycles per second (Hz). It is then natural that oscillators should be often classified according to their band of operational frequencies.

The phase shift oscillator is one such oscillator that falls under the class of harmonic oscillators producing sine waves and it is usually suitable for applications in the GPS, musical instruments and voice synthesis.

Expected Skills

After performing this experiment, you would be able to:

- ❖ state the Barkhausen criterion which should be fulfilled to produce sustained oscillations;
- ❖ describe how feedback can be used to convert an amplifier into an oscillator;
- ❖ draw the circuit of a phase shift oscillator and explain how an R - C section produces a phase shift between its input and output;
- ❖ design a phase shift oscillator of given frequency; and
- ❖ build the circuit of a phase shift oscillator and measure its output frequency.

You will require the following apparatus to perform this experiment.

Apparatus Required

IC 741C, dual power supply (± 15 V), 3 sets of equal value resistors and capacitors, a high value feedback resistor, dual trace oscilloscope (CRO), breadboard, connecting wires.

10.2 PHASE SHIFT OSCILLATOR FUNDAMENTALS

10.2.1 Phase Shift

Any complex electric signal can be visualised as a combination of several sinusoidal waves with differing amplitudes, frequencies and phases. A single sine wave has three attributes associated with it – its amplitude (voltage / current), frequency and the phase. Out of these three attributes, the first two are *absolute* whereas the third – the phase needs a *reference* wave. A *reference* sinusoidal wave may always be mathematically represented by an equation such as

$$v = V_m \sin(\omega t) \quad (10.1)$$

where v is the instantaneous value of varying voltage, V_m the amplitude and ω the angular frequency. If we generate another independent sine wave after a quarter cycle of this wave is over with the same amplitude and frequency, it would have an expression $v = V_m \sin(\omega t + 90^\circ)$ since a quarter cycle corresponds to one-fourth of 360° . Since $\sin(A + 90^\circ) = \cos A$, the second waveform now can be written as $v = V_m \cos(\omega t)$. Two such waves with a phase difference of 90° after setting their amplitudes and frequencies equal are shown in Fig.10.1.

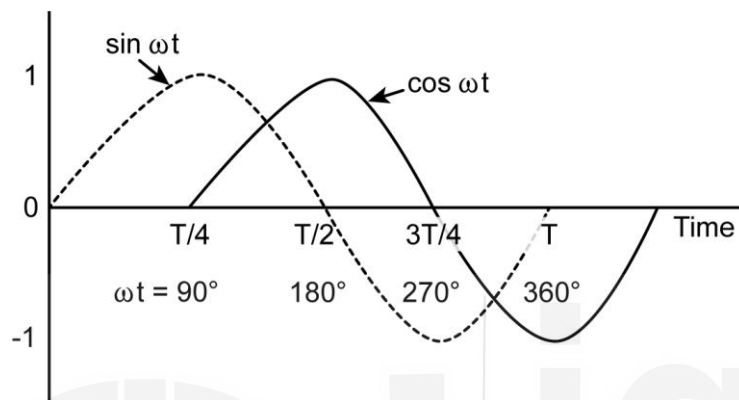


Fig.10.1: Two waves differing in phase by 90° ($\frac{\pi}{2}$ radians) can be represented by sine and cosine functions.

In general, any sinusoidal voltage waveform may be expressed as $v = V \sin(\omega t + \phi)$ where ϕ represents the phase angle with reference to an arbitrary zero.

In an R - C circuit (or even R - L circuit), there exists a phase difference ϕ between the applied voltage and consequent electric current through components due to the ability of capacitor /inductor to store energy. This is evident directly from the basic capacitor equation too.

You know that, by definition, capacitance $C = Q/v$ where Q is the charge on the capacitor and v is the reference voltage. Hence, we have $Q = v.C$ and therefore, by definition, the expression for the current through the capacitor is

$$i = \frac{dQ}{dt} = C \frac{dv}{dt} = C\omega V_m \cos(\omega t) \quad (10.2)$$

It is therefore evident that the phase shift in a purely capacitive circuit is $\phi = 90^\circ$. However, in an R - C circuit, due to the resistive component of total impedance of the circuit, the **phase shift** would be always less than 90° and given by

$$\phi = \tan^{-1}\left(\frac{X_C}{R}\right) \quad (10.3)$$

where X_c is the capacitive reactance and equals $1/(2\pi fC)$.

If we cascade several R - C sections with same values of components as shown in Fig. 10.2, it is possible to create phase differences of any value between 0° and 360° .

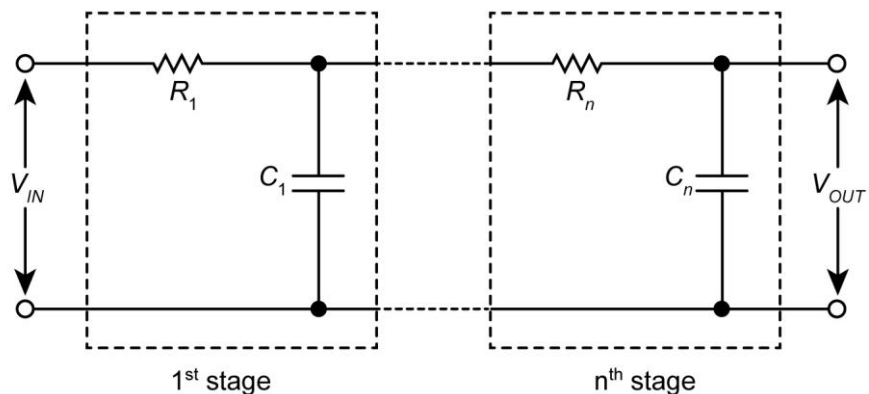


Fig.10.2: Cascading of n R - C sections for obtaining desired phase shift.

This fact is used in converting an amplifier into a phase shift oscillator. Usually an inverting amplifier made using transistor or an operational amplifier is used for the purpose. For this to happen, there are certain conditions to be fulfilled. Together, they are called the Barkhausen criterion.

The Barkhausen criterion for sustained oscillations states that:

- The phase shift *around the loop* is an integral multiple of 360° .
- The loop gain is equal to unity in absolute magnitude, i.e., $|\beta A| = 1$.

You must note here that, Barkhausen is an essential but not the sufficient condition for oscillations to occur and sustain in electronic circuits – there are circuits that don't oscillate even after satisfying the criterion. Further, the criterion neither speaks about the type of amplifier nor the mechanism which provides the frequency-dependent feedback.

10.2.2 Phase Shift Oscillator Circuit

A popular circuit of a phase-shift oscillator which makes use of the commonly available operational amplifier IC741 is shown in Fig.10.3. The prime reason why we chose this circuit is that although an inverting amplifier could be assembled using a BJT or an FET (see the circuits shown in Fig. 10.4a and b), such amplifiers do not exhibit the close proximity that an op amp exhibits as a perfect/ideal amplifier. As such, the deviation in the observed and expected frequency of the oscillator could be larger. Also, the availability of economical operational amplifiers is much better than conventional transistors.

The circuit in Fig.10.3 uses three RC sections that create **a phase lead of about 60° each** but if the positions of R and C are interchanged, the circuit works equally well creating phase lag around the three RC sections.

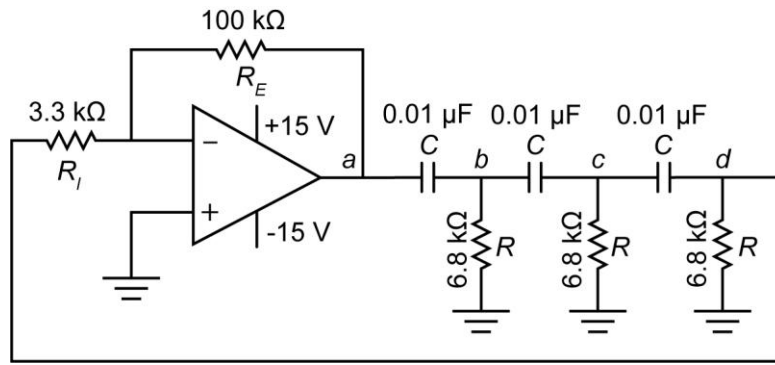


Fig.10.3: Phase shift oscillator employing an Operational amplifier IC 741.

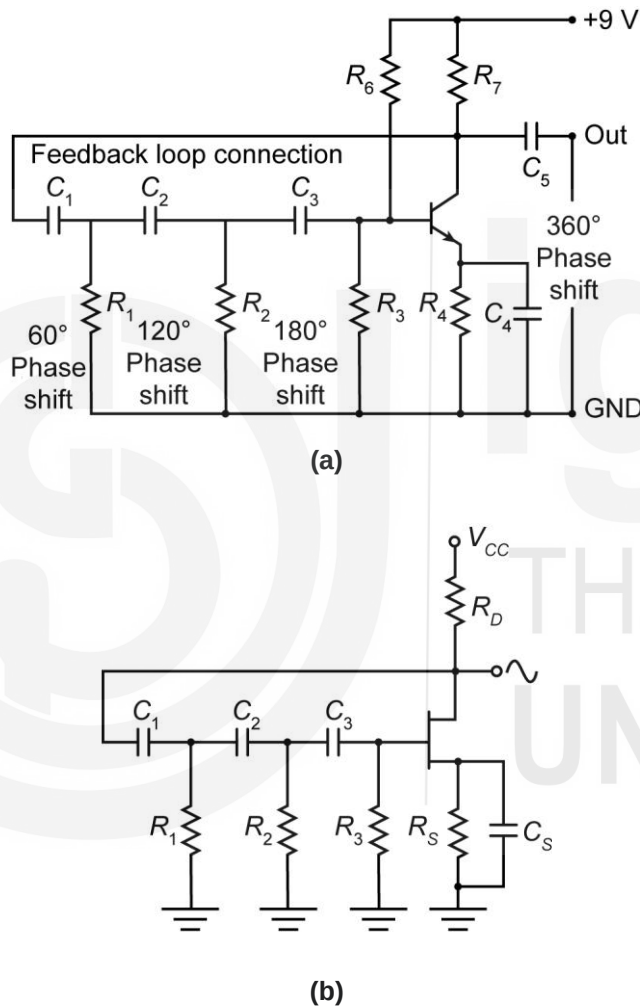


Fig. 10.4: Phase shift oscillator employing a) an *n-p-n* transistor; b) a JFET

As the operational amplifier has a dual power supply, it can provide a zero-centred output ac sinusoidal waveform. The op amp has been configured in the inverting mode. It has an open loop gain equal to $[-R_E/R_I]$.

The operational amplifier makes use of a feedback resistance of about $100\text{ k}\Omega$ such that in conjunction with its input resistor of $3.3\text{ k}\Omega$, it can provide an loop gain of over -30 . This is essential since at the resonant frequency when the cluster of three R - C sections provides a phase shift of exact 180° , the output across the rightmost resistor is about $1/29$ of that at the input of the left-most RC section between point 'a' and ground. Only with a gain of slightly more

than 29, the closed loop gain can become unity and the oscillations sustain. This can be derived using a Kirchhoff's network rules, but is beyond the scope of our discussion here.

The frequency of the oscillations is controlled by the values of R and C . When we choose equal values of resistors and capacitors for all the *three* sections, the frequency is given by

$$f = \frac{1}{2\pi RC\sqrt{6}} \quad (10.4)$$

If the number of RC sections is n , the general formula is

$$f = \frac{1}{2\pi RC\sqrt{2n}} \quad (10.4a)$$

You can calculate that for the suggested component values in Fig.10.3, the frequency would be about 1 kHz.

10.3 BUILDING AND TESTING A PHASE SHIFT OSCILLATOR

1. Build the phase shift oscillator by assembling the circuit shown in Fig. 10.3 using a breadboard. You should use a combination of three fixed value resistors $3.3\text{ k}\Omega$ and capacitors $0.01\mu\text{F}$ (suggested) in the R - C network. Use a $100\text{ k}\Omega$ potentiometer as the feedback resistor in the inverting amplifier so that the gain can be adjusted to watch oscillations appear and disappear according to the compliance of Barkhausen conditions stated earlier.
2. Take a dual channel oscilloscope (CRO) and connect the output of your circuit (pin 6 of op amp) to one of its channels. With this you will be able to observe the sinusoidal waveform output of your circuit.
3. Keep the probe of second channel of the CRO free, with which you can touch various points in the circuits manually, and observe the waveforms available at those points. With this arrangement, it becomes possible to watch the phase changes as the output signal passes successively from one R - C section to another (respectively between points a - b - c - d and common ground of the circuit).
4. You should make the frequency measurement carefully by stabilizing the output waveform to see only about one complete cycle on the CRO display screen.
5. Measure the time period of one cycle of the wave by noting the wavelength reading on the time axis and multiplying it by the chosen time base (Time/Div) setting. Record your observations in Observation Table 10.1.

6. Compute the frequency most correctly by using the relation ($f = 1/T$).
7. Compare the observed frequency with the expected frequency calculated from the component values and calculate the error. .
8. Change the combination of R and C values to get four more frequency values and repeat steps 4 to 7 in each case.
9. Trace the waveform obtained on the CRO screen on a tracing paper and note the V/cm and Time/Div settings chosen for that measurement.

Observation Table 10.1: Frequency of a phase shift oscillator

Sl. No.	R (Ω)	C (μF)	Wavelength on CRO screen (cm)	Time base setting of oscilloscope (ms or μs) / Div	Period of wave T(s)	Frequency, $f = 1/T$ (Hz)
1						
..						
5						

You may create another Table to determine the error in the measurement as suggested below.

Table 10.2: Error Analysis

Sl. No.	R (Ω)	C (μF)	Expected frequency $f = \frac{1}{2\pi RC\sqrt{6}}$ (Hz)	Observed frequency f_{obs} (Hz)	Difference in frequency $\delta = f - f_{obs}$ (Hz)	% error = $[\delta/f] * 100$
1						
..						
5						

Conclusions

Compare the expected and observed values of frequencies and check how well they match.

Comment on the quality of sine waveform you have obtained in each set of your observation.

SAQ 1 - Analysis of phase shift oscillator measurements

- a) If there is a difference between the expected and observed values of frequency values, what could be the reasons for this deviation?
 - b) What will be the formula for expected frequency, if you use 4 stage of *R-C* network in your circuit? What will be the phase shift per stage in this case?
-

